IRS44273LTRPBF-TP

Single-Channel, High-Speed, Low-side Gate Driver

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Features

- 4.5 to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO
- TTL and CMOS Compatible Input-Logic Threshold
- Input Design Output Held Low when Input Pins are Floating
- Fast Rise and Fall Times (9ns and 7ns typical)
- Fast Propagation Delays (13ns typical)
- Split Output Configuration
- Strong Sink Current Offers Enhanced Immunity Against Miller Turn on
- Input Pins Capable of Withstanding - 5 V Below GND pin
- Compact package: SOT23-5

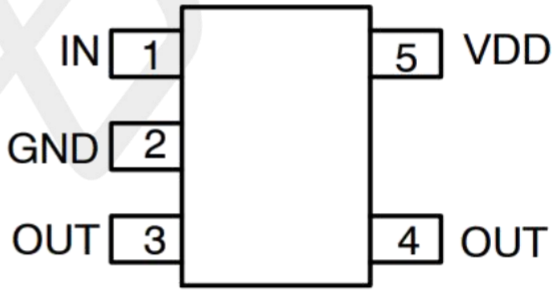
General Description

The device is a compact gate driver that offers superior replacement of NPN and PNP discrete driver (buffer circuit) solutions. driver rated for MOSFETs, IGBTs, and emerging wide-bandgap power devices such as GaN. suitable for high-speed applications. Its asymmetrical 4-A peak source and 8-A peak sink currents boost immunity against parasitic Miller turn on effect. Features including wide input hysteresis and negative input voltage handling enhance transient immunity.

Applications

- DC-to-DC Converters
- Desktop PC Power
- Switch-Mode Power Supplies
- Companion Gate-Driver Devices for Digital Power Controllers
- Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)

Pin out (top view)



Pin Configurations

Pin	Name	Function
1	IN	Non-inverting Input
2	GND	Ground,Common ground reference for input and output circuits.
3	OUT	Gate Drive Output.
4	OUT	Gate Drive Output.
5	VDD	Supply Voltage，

Absolute Maximum Ratings (Note1)

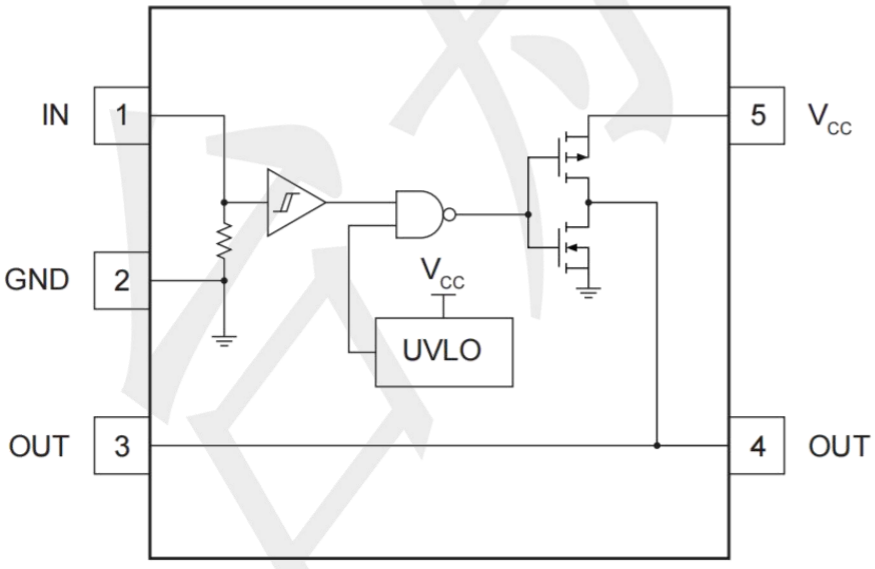
Description	Min	Max	Unit
Supply Voltage, VDD	-0.3	20	V
Output Voltage, OUT	-0.3	20	V
Input, IN	-6.0	20	V
Output continuous source current	0.3		A
Output continuous sink current	0.6		A
Output pulsed (0.5us) source current	4.0		A
Output pulsed (0.5us) sink current	8.0		A
Junction Temperature	125		°C
Storage Temperature	-40	150	°C
Lead Temperature (Soldering, 10s)	300		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Recommended Operating Conditions

Description	Min	Max	Unit
Supply Voltage, VDD	4.5	18	V
Input, IN	-5.0	18	V
Operating Junction Temperature	0	125	°C

Internal Block Diagram



OUTPUT LOGIC

IN	OUT
0	0
1	1
X	0

X = Floating Condition

Electrical Characteristics (VDD=12V, T_J=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Startup Current	I_{START}	VDD=3.4V,IN+=VDD, IN-=GND	40	100	160	uA
		VDD=3.4V, IN+=IN-=GND	25	75	145	
		VDD=3.4V,IN+=GND, IN-=VDD	20	60	115	
VDD Start Threshold	V_{ON}	V_{IN} = 4V to 36V	3.9	4.2	4.5	V
VDD OFF Threshold	V_{OFF}		3.0	3.5	4.0	V
VDD Hysteresis	V_{HYS}			0.7		V
Input Signal High Threshold	$V_{H(IN)}$		--	2.4	2.6	V
Input Signal Low Threshold	$V_{L(IN)}$		1.0	1.2	--	V
Source Peak Current	I_{PSRC}	C_{load}=0.22uF, f_S=1kHz	--	-4	--	A
Sink Peak Current	I_{PSNK}	C_{load}=0.22uF, f_S=1kHz	--	8	--	A
High Output Voltage	V_{OH}	VDD=12V, I_{OUTH}= -10mA	--	50	90	mV
		VDD=4.5V, I_{OUTH}= -10mA	--	60	130	mV
Low Output Voltage	V_{OL}	VDD=12V, I_{OUTL}= 10mA	--	5	6.5	mV
		VDD=4.5V, I_{OUTL}= 10mA	--	5.5	10	mV
Output Pullup Resistance	R_{OH}	VDD=12V, I_{OUTH}= -10mA	--	5	7.5	Ω
		VDD=4.5V, I_{OUTH}= -10mA	--	5	11	Ω
Output Pulllow Resistance	R_{OL}	VDD=12V, I_{OUTL}= 10mA	--	0.375	0.65	Ω
		VDD=4.5V, I_{OUTL}= 10mA	--	0.45	0.75	Ω
Rise Time	T_{RISE}	VDD=12V,C_{LOAD}=1.8nF,OUTH, OUTL tied together	--	8	12	nS
		VDD=4.5V,C_{LOAD}=1.8nF,OUTH, OUTL tied together	--	16	22	nS
Fall Time	T_{FALL}	VDD=12V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	--	7	11	nS
		VDD=4.5V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	--	7	11	nS
IN+ to output propagation delay	T_{DELAY+}	VDD=12V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	9	23	33	nS
		VDD=4.5V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	9	25	36	nS
IN- to output propagation delay	T_{DELAY-}	VDD=12V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	9	23	33	nS
		VDD=4.5V,C_{LOAD}=1.8nF, OUTH, OUTL tied together	9	29	40	nS

Typical Characteristics (VDD=12V, T_J=25℃, unless otherwise specified)

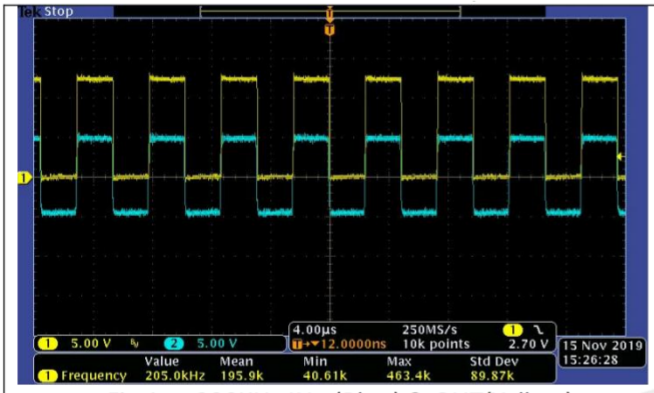


Fig 1. 200KHz IN+ (Blue) & OUT(Yellow)

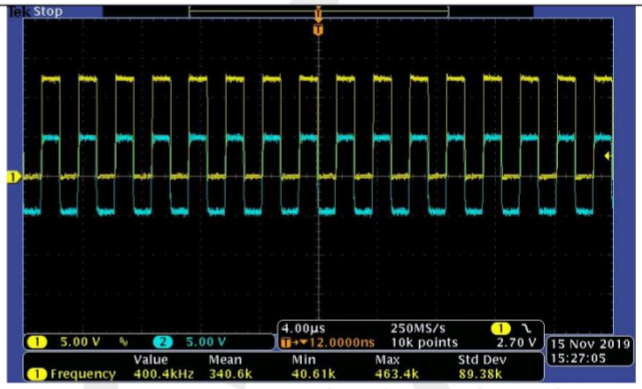


Fig 2. 400KHz IN+ (Blue) & OUT(Yellow)

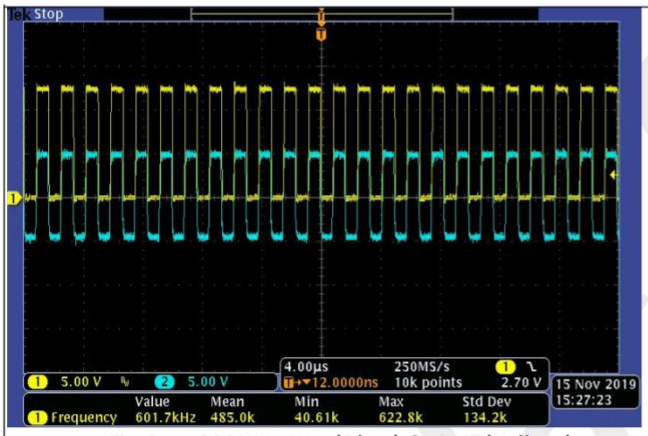


Fig 3. 600KHz IN+ (Blue) & OUT(Yellow)

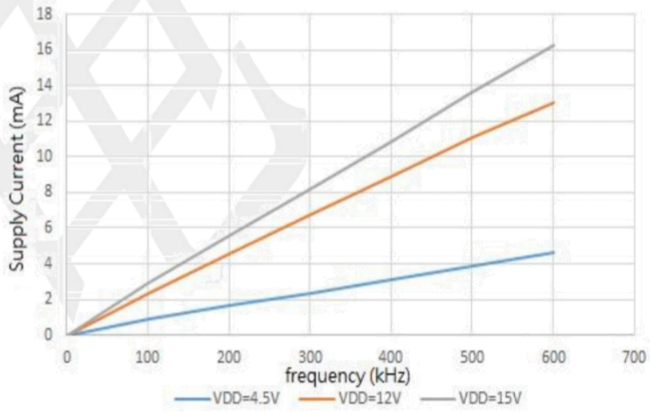
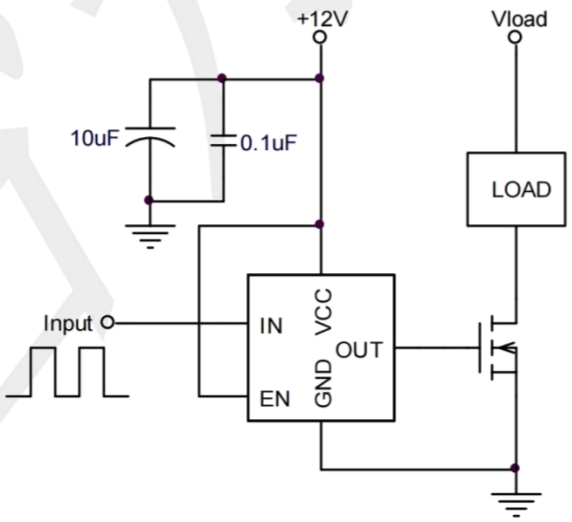


Fig 4. Supply Current vs Frequency

Typical Application Circuit



IC Operation Information

Basic Operation

The single-channel high-speed low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical).

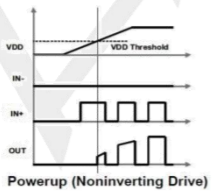
For system robustness, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.
is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

VDD and Undervoltage Lockout

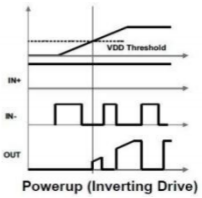
The device has internal Undervoltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when VDD voltage less than VON during power up and when VDD voltage is less than VOFF during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis prevents chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in IDD. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide band-gap power-semiconductor devices.

For example, at power up, the driver output remains LOW until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD until steady-state VDD is reached. In the noninverting operation (PWM signal applied to IN+ pin) shown in Figure, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown in Figure the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high state only if IN pin is high and after the UVLO threshold is reached.

Since the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD-bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.



Powerup (Noninverting Drive)



Powerup (Inverting Drive)

Operating Supply Current

The feature very low quiescent IDD currents. The typical operating-supply current in Undervoltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized. The IDD current when the device is fully on and outputs are in a static state (DC high or DC low) represents lowest quiescent IDD current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent IDD current, the average IOUT current due to switching, and finally any current related to pullup resistors on the unused input pin. For example, when the inverting input pin is pulled low additional current is drawn from VDD supply through the pullup resistors (refer to for the device Block Diagram). Knowing the operating frequency (fSW) and the MOSFET gate (QG) charge at the drive voltage being used, the average IOUT current can be calculated as product of QG and fSW.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8nF switching load is provided. The strikingly linear variation and close correlation with theoretical value of average IOUT indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

Input Stage

The input pins of the deviceis based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With a typically high threshold of 2.2 V and a typically low threshold of 1.2 V, the logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (1 V typical) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V.This device also features tight control of the input-pin threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The very-low input capacitance on these pins reduces loading and increases switching speed.

Whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This function is achieved using VDD-pullup resistors on all the inverting inputs (IN– pin) or GND-pulldown resistors on all the noninverting input pins (IN pin), (see the).

Enable Function

As mentioned earlier, an enable and disable function is easily implemented in a devices using the unused input pin. When the IN pin is pulled down to GND , the output is disabled. Thus the IN pin can be used like an enable pin that is based on active-high logic.

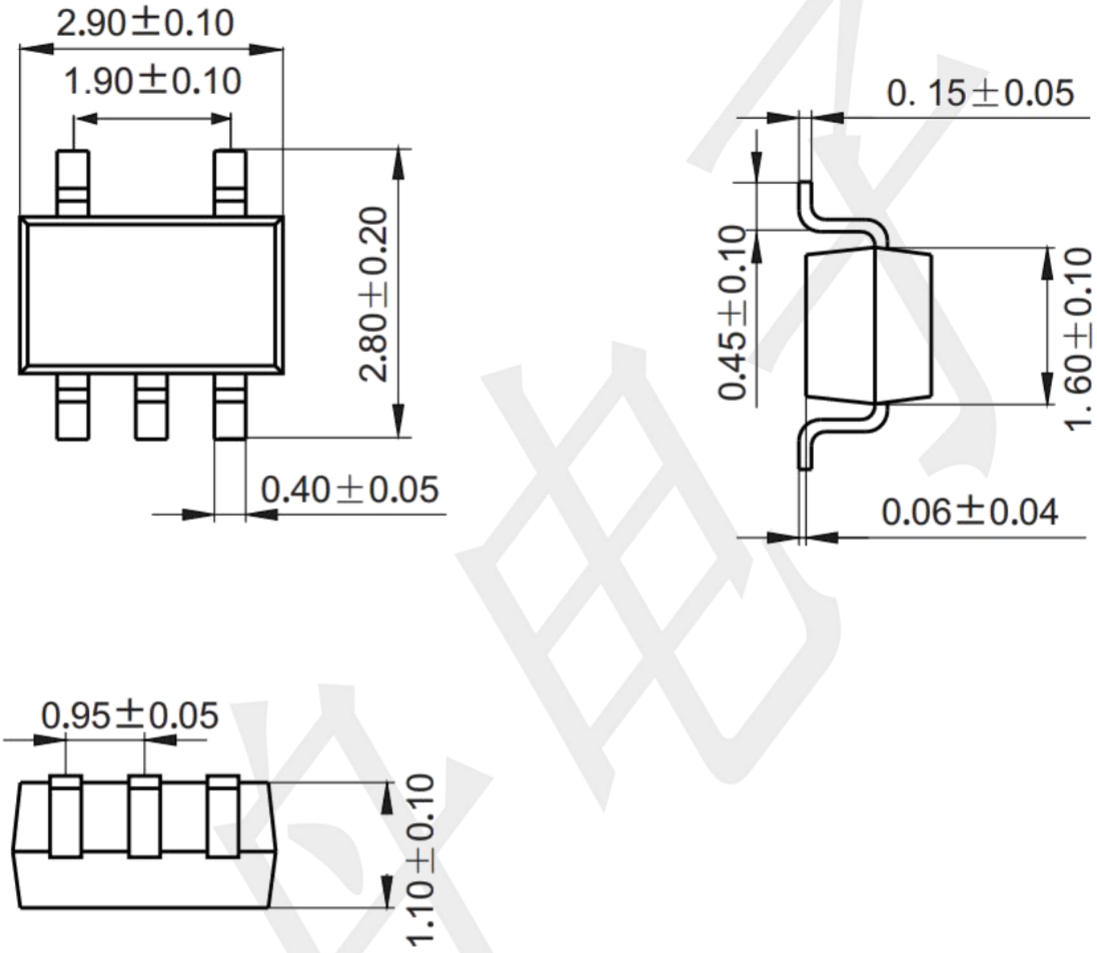
Output Stage

Here shows the output stage of the devices. The devices feature a unique architecture on the output stage which delivers the highest peak-source current when the peak source current is most needed during the Miller plateau region of the power switch turn on transition (when the power-switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

The RO parameter is a DC measurement and is representative of the on-resistance of the P-channel device only, because the N-Channel device is turned on only during output change of state from low to high.

Package Outline Dimensions (unit: mm)

SOT23-5



Mounting Pad Layout (unit: mm)