

General Description

The WSP3099 is the highest performance trench P-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSP3099 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

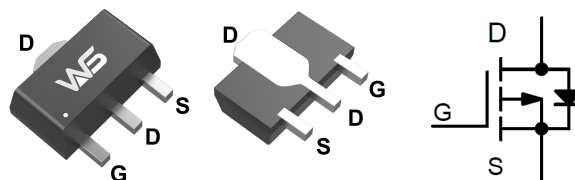
Product Summery

BVDSS	RDSON	ID
-30V	53mΩ	-5.0A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-89 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-5.0	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-4.0	A
I_{DM}	Pulsed Drain Current ²	-20	A
EAS	Single Pulse Avalanche Energy ³	18	mJ
I_{AS}	Avalanche Current	8	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	1.8	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62.5	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	30	$^{\circ}C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.02	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-5.0A	---	53	65	mΩ
		V _{GS} =-4.5V, I _D =-3.8A	---	80	98	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	-1.5	-2.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.32	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	5.5	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	24	48	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-5A	---	11.6	---	nC
Q _{gs}	Gate-Source Charge		---	1.3	---	
Q _{gd}	Gate-Drain Charge		---	2.5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GEN} =-10V, R _G =3.3Ω I _D =-1A, R _L =15Ω	---	6	12	ns
T _r	Rise Time		---	12	23	
T _{d(off)}	Turn-Off Delay Time		---	25	46	
T _f	Fall Time		---	6	12	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	625	---	pF
C _{oss}	Output Capacitance		---	100	---	
C _{rss}	Reverse Transfer Capacitance		---	60	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =25V, L=0.1mH, I _{AS} =6A	6	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	-2.0	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	-20	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1.7A, T _J =25°C	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-6A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

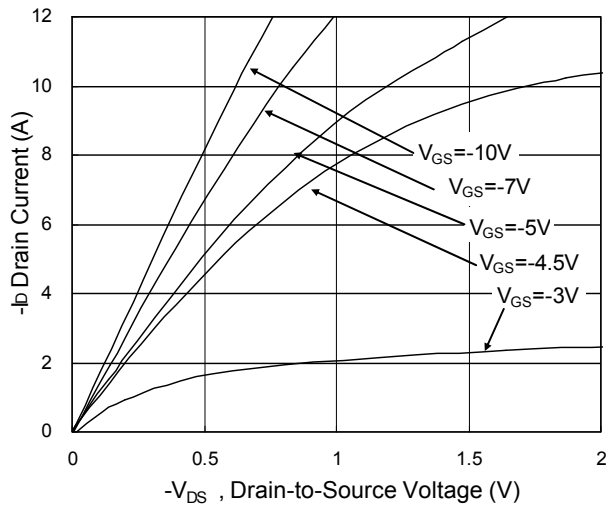


Fig.1 Typical Output Characteristics

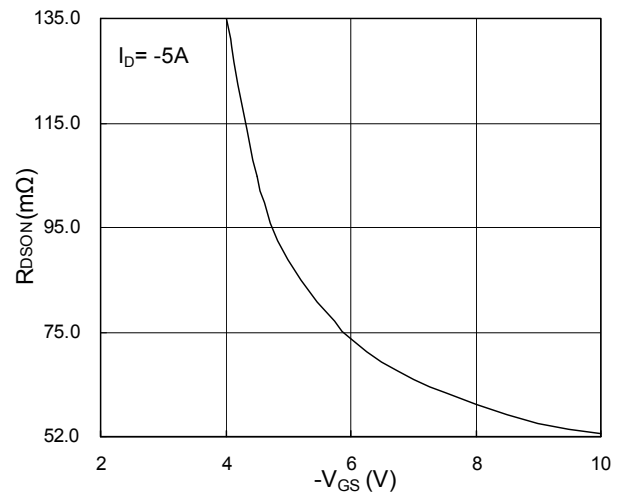
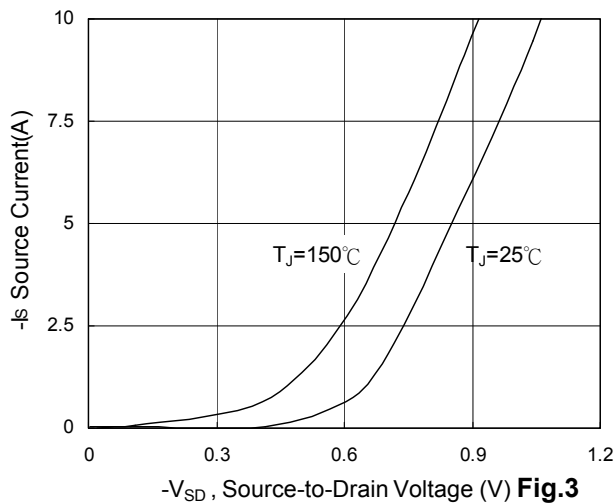


Fig.2 On-Resistance vs. G-S Voltage



Forward Characteristics of Reverse

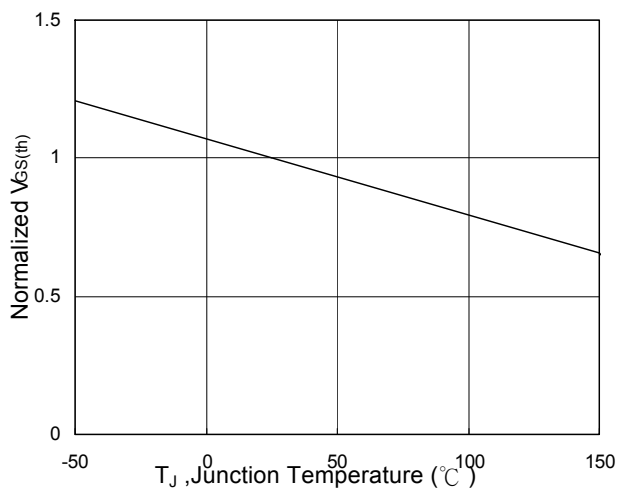


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

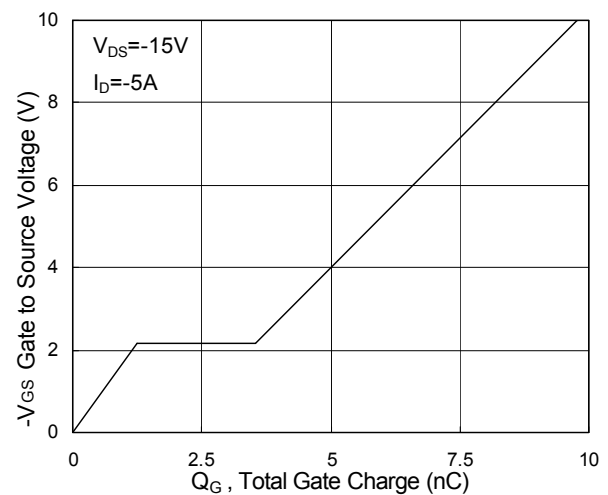


Fig.4 Gate-Charge Characteristics

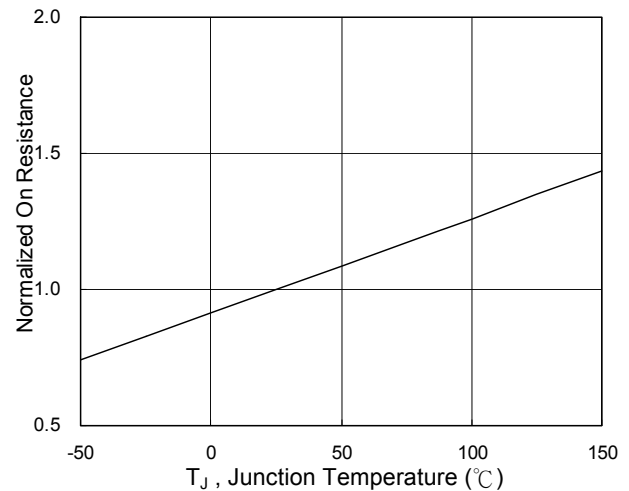


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

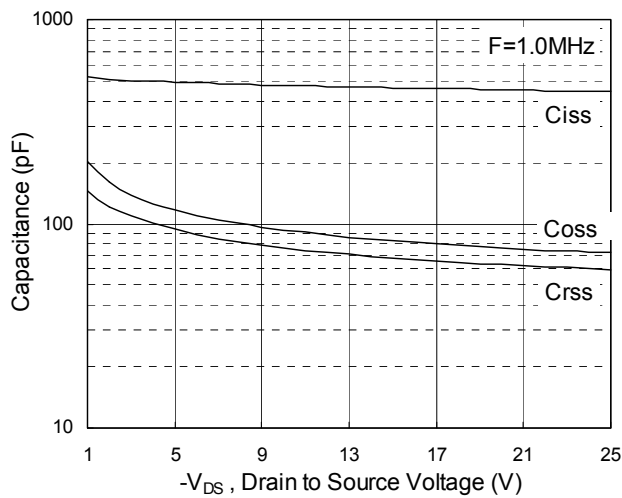


Fig.7 Capacitance

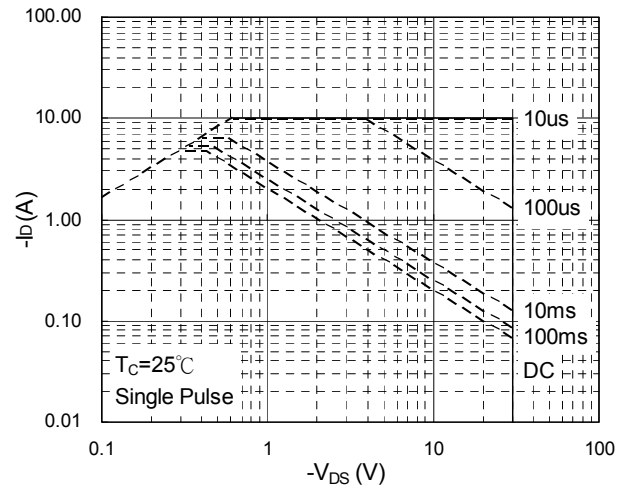


Fig.8 Safe Operating Area

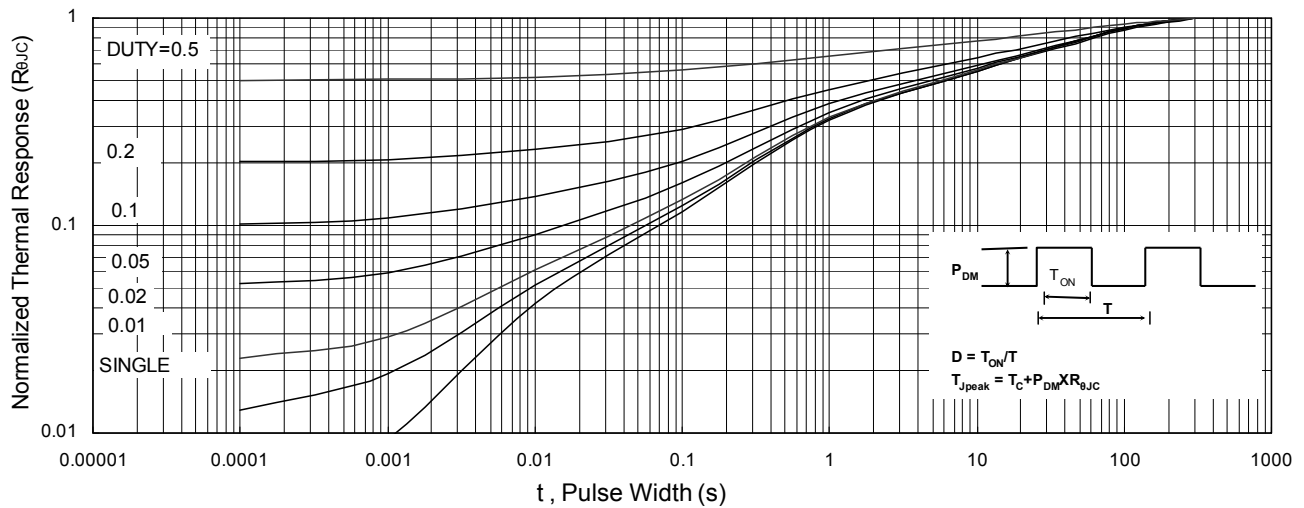


Fig.9 Normalized Maximum Transient Thermal Impedance

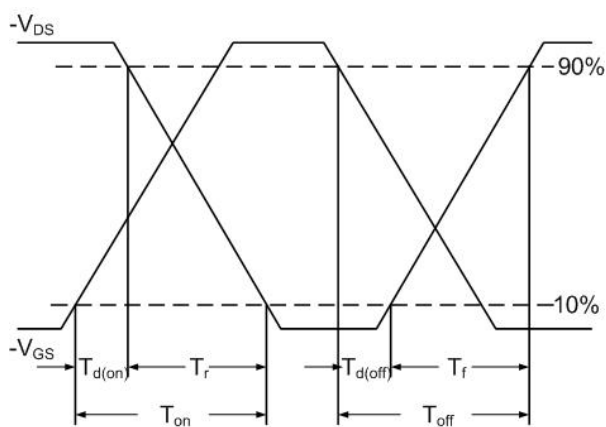


Fig.10 Switching Time Waveform

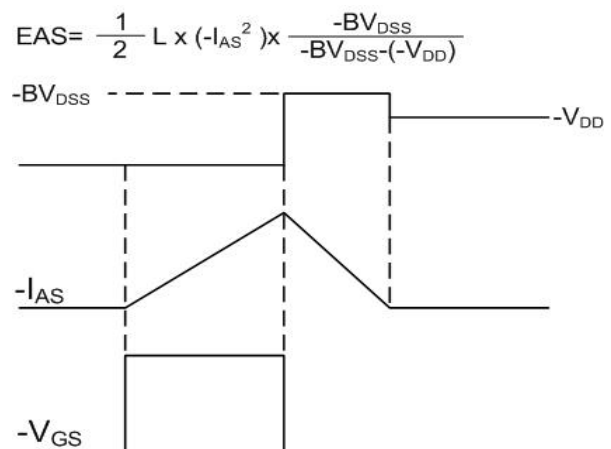


Fig.11 Unclamped Inductive Waveform

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