

General Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

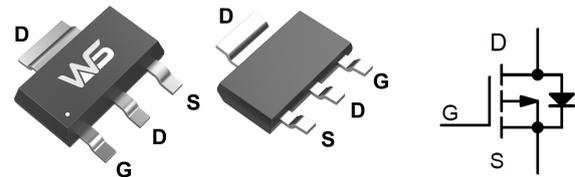
Product Summary

BVDSS	RDS(on)	ID
-60V	215mΩ	-2A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter.
- Networking DC-DC Power System
- Load Switch

SOT-223 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-1.6	A
I_{DM}	Pulsed Drain Current	-10	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case	---	5.4	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-60	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.03	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-2A	---	175	215	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	205	260	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	-1.9	-3.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.56	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-60V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-60V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-15V, I _D =-2A	---	5	---	S
Q _g	Total Gate Charge	V _{DS} =-48V, V _{GS} =-4.5V, I _D =-1A	---	6.3	---	nC
Q _{gs}	Gate-Source Charge		---	2.3	---	
Q _{gd}	Gate-Drain Charge		---	1.8	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-30V, V _{GS} =-10V, R _{GEN} =3.3Ω, RL=30Ω.	---	20	---	ns
T _r	Rise Time		---	3	---	
T _{d(off)}	Turn-Off Delay Time		---	5.2	---	
T _f	Fall Time		---	3.8	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	364	---	pF
C _{oss}	Output Capacitance		---	41	---	
C _{rss}	Reverse Transfer Capacitance		---	12	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	-2	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =-1.2A, T _J =25°C	---	---	-1.2	V

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: The power dissipation PD is based on T_{J(MAX)}=150°C, u s i n g ≤10s junction-to-ambient thermal resistance.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJA} and lead to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

Typical Characteristics

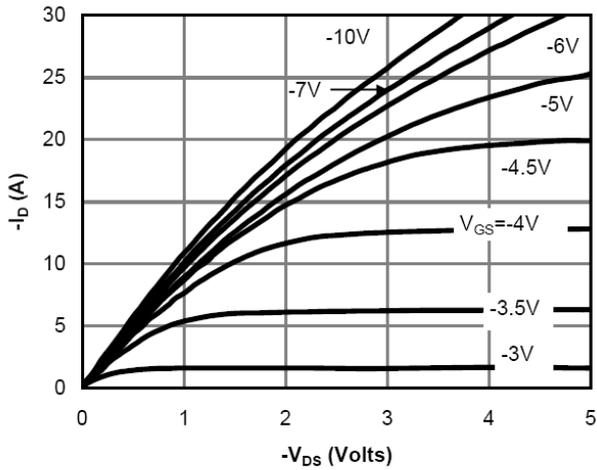


Fig 1: On-Region Characteristics

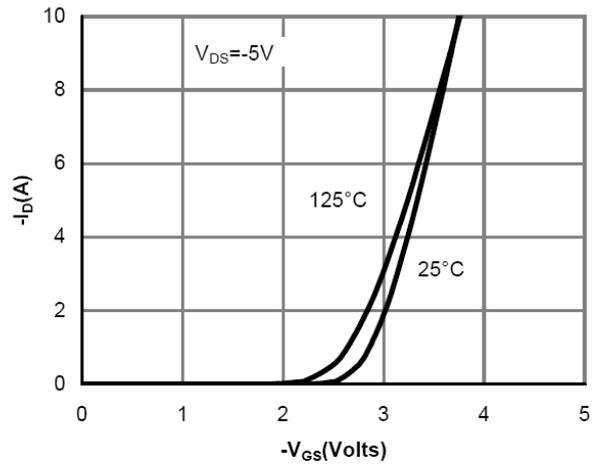


Figure 2: Transfer Characteristics

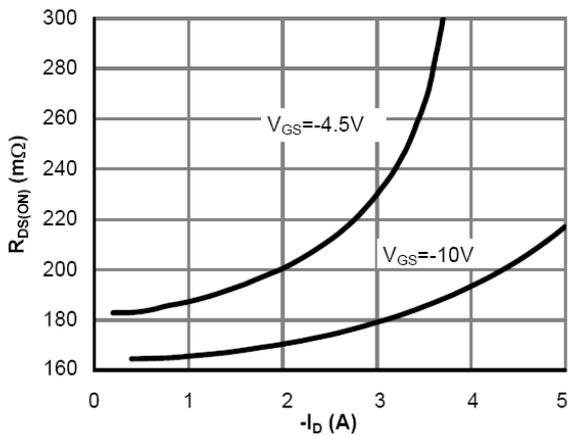


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

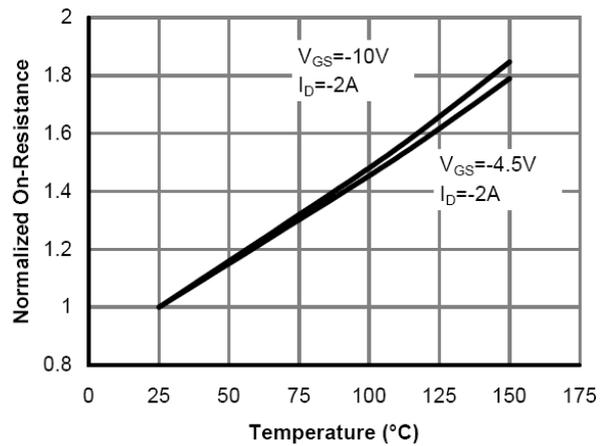


Figure 4: On-Resistance vs. Junction Temperature

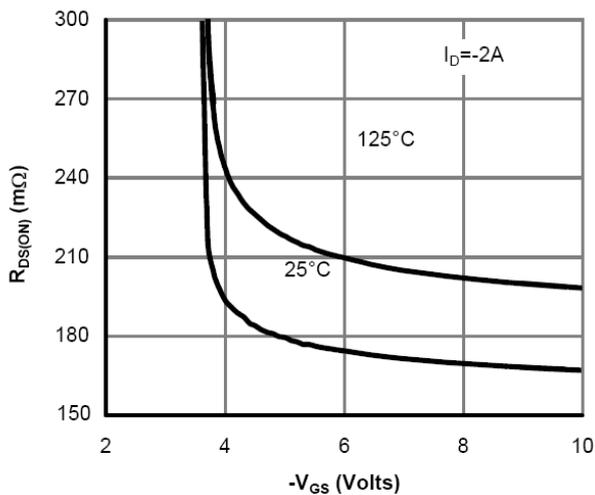


Figure 5: On-Resistance vs. Gate-Source Voltage

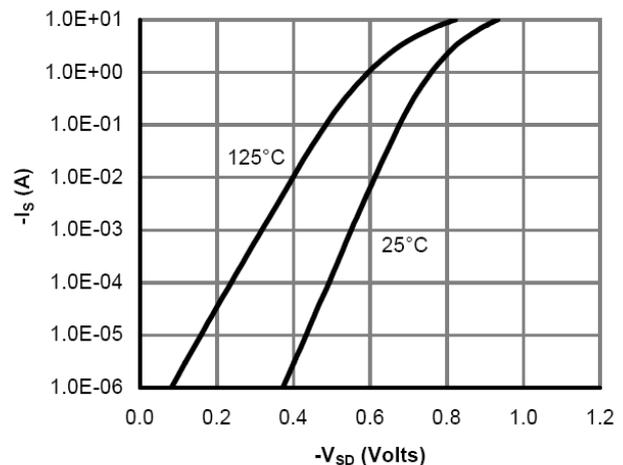


Figure 6: Body-Diode Characteristics

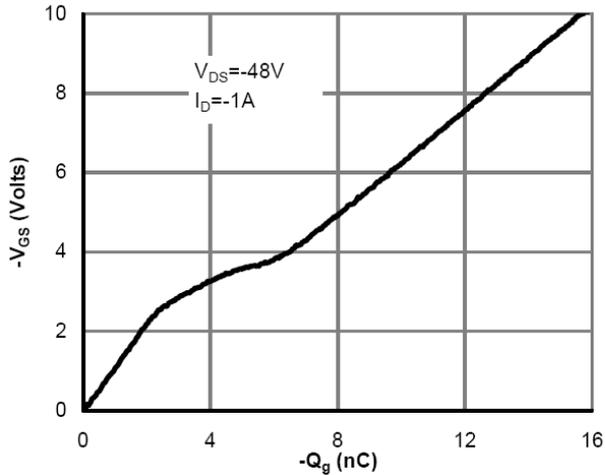


Figure 7: Gate-Charge Characteristics

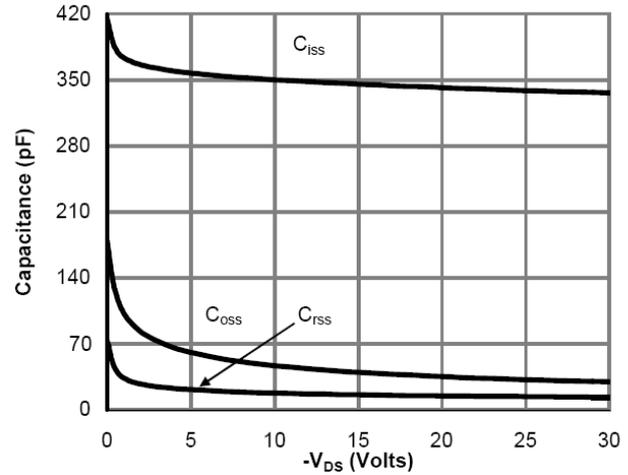


Figure 8: Capacitance Characteristics

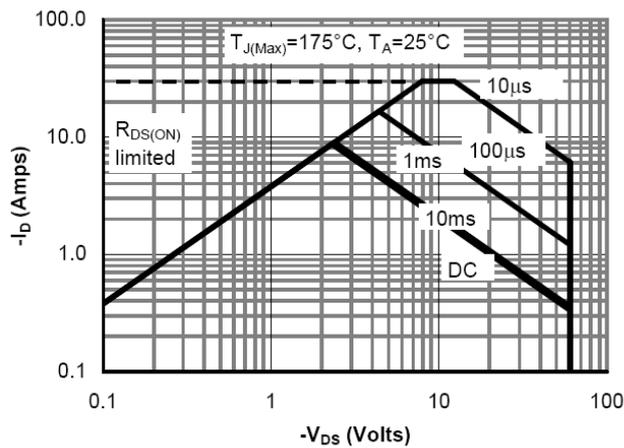


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

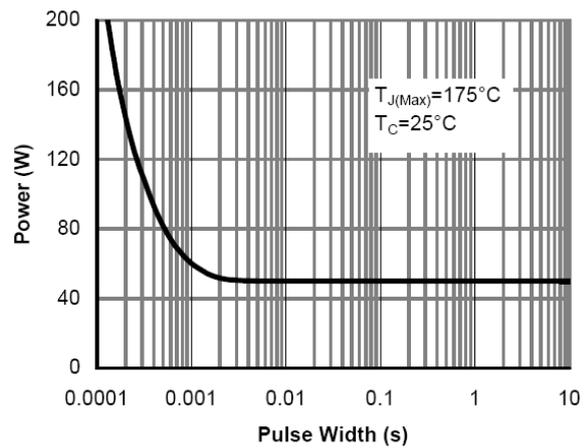


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

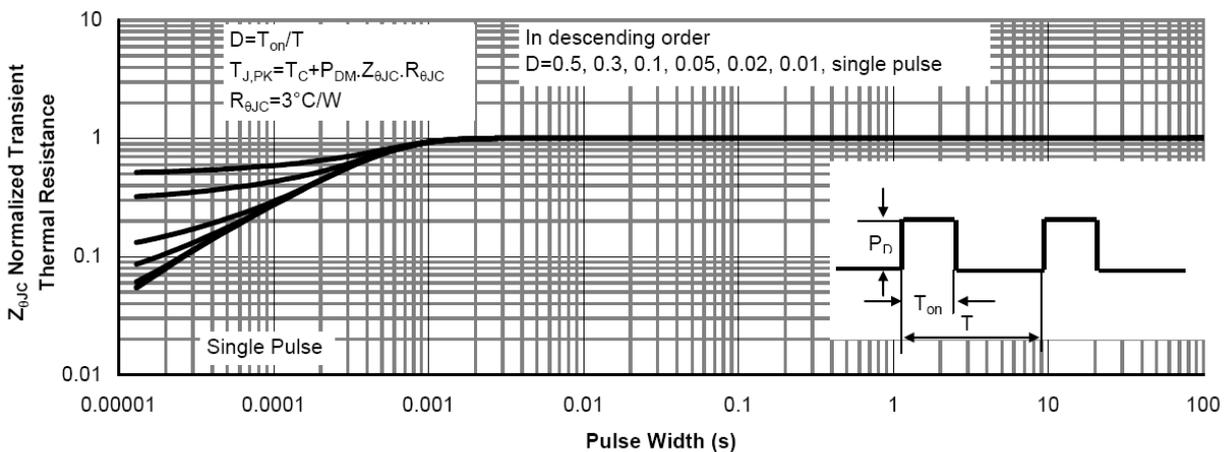


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



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