WST3392

Dual N-Ch MOSFET

General Description

The WST3392 is the highest performance trench Dual N-ch MOSFETs with extreme high cell density , which provide excellent R_{DSON} and gate charge for most of the small power switching and load switch applications.

The WST3392 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

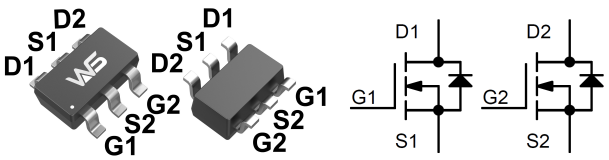
Product Summery

BVDSS	RDSON	ID
30V	40mΩ	3.7A

Applications

- Power management in portable and battery operated products
- One cell battery pack protection

SOT-23-6L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	3.7	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	3.0	A
I_{DM}	Pulsed Drain Current[2]	20	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.15	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	110	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	80	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.028	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=3.5A	---	40	50	mΩ
		V_{GS}=6V , I_D=2A	---	45	65	
		V_{GS}=4.5V , I_D=2A	---	58	73	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-3.21	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=30V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=30V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=5A	---	12	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	4	6	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=10V , I_D=3.5A	---	4.05	5	nC
Q_{gs}	Gate-Source Charge		---	0.55	0.8	
Q_{gd}	Gate-Drain Charge		---	1.0	1.8	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GEN}=10V , R_G=3Ω I_D=1.0A ,R_L=4.2Ω.	---	4.5	---	ns
T_r	Rise Time		---	1.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	18.5	---	
T_f	Fall Time		---	15.5	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	170	210	pF
C_{oss}	Output Capacitance		---	35	45	
C_{rss}	Reverse Transfer Capacitance		---	23	30	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	1.5	A
I_{SM}	Pulsed Source Current[2,4]		---	---	3.5	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_{SD}=3.5A , T_J=25℃	---	---	1.0	V
t_{rr}	Reverse Recovery Time	I_F=3.5A,dI/dt=100A/μs , T_J=25℃	---	7.5	---	nS
Q_{rr}	Reverse Recovery Charge		---	2.5	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

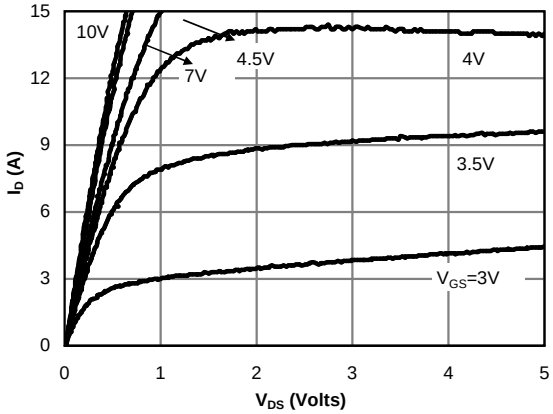


Fig 1: On-Region Characteristics (Note E)

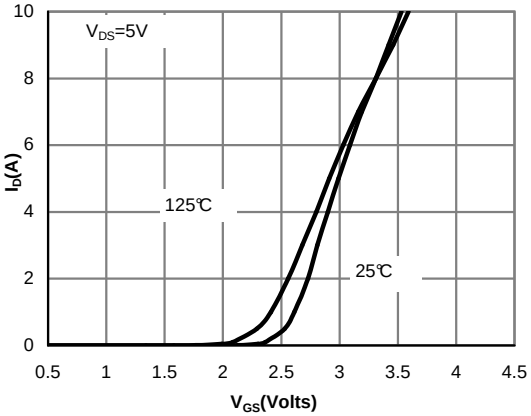


Figure 2: Transfer Characteristics (Note E)

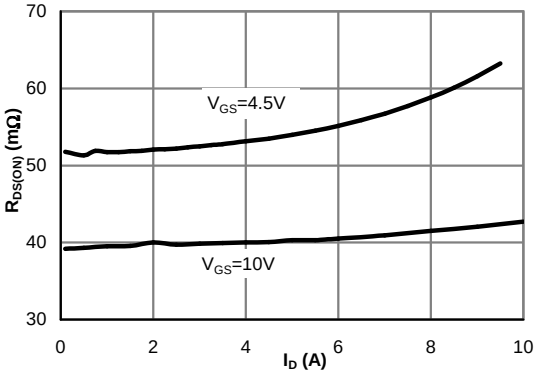


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

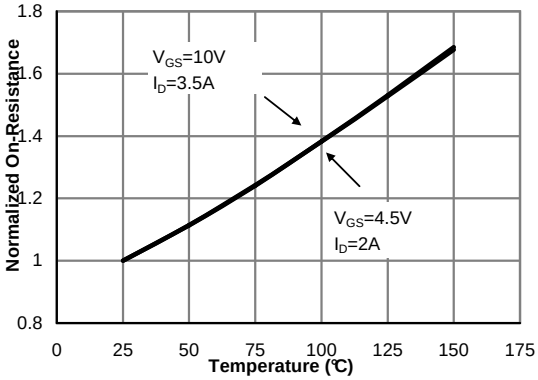


Figure 4: On-Resistance vs. Junction Temperature (Note E)

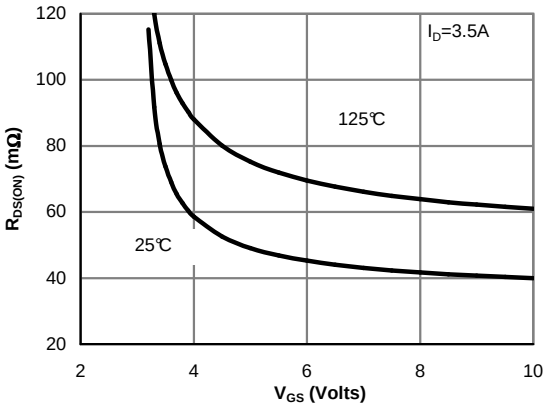


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

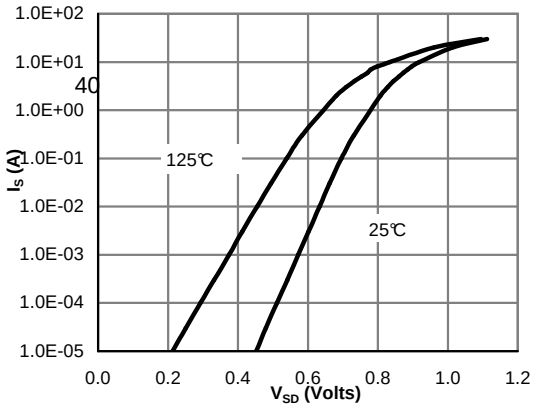


Figure 6: Body-Diode Characteristics (Note E)

Typical Characteristics

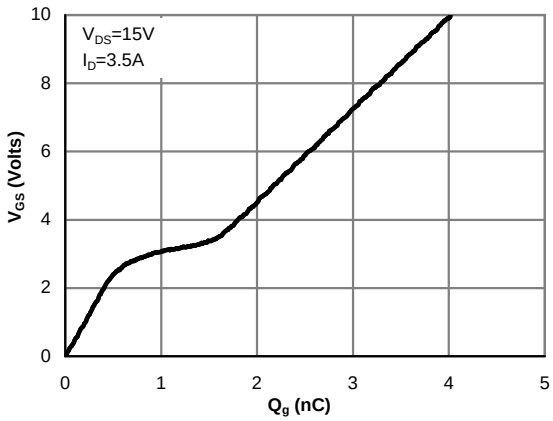


Figure 7: Gate-Charge Characteristics

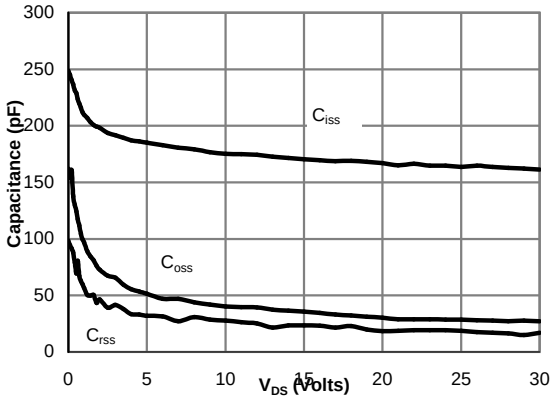


Figure 8: Capacitance Characteristics

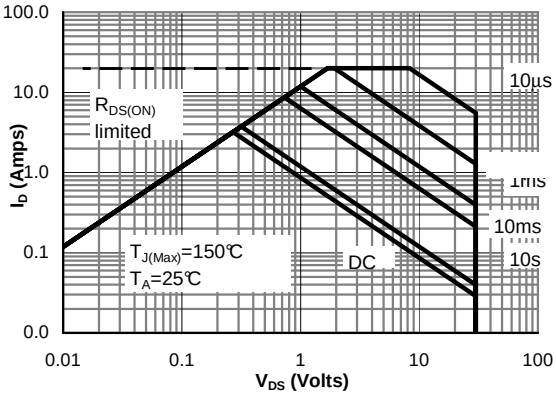


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

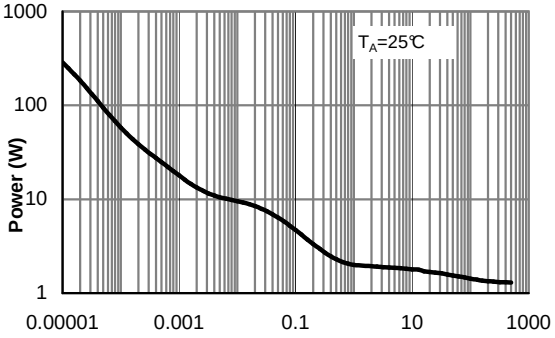


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

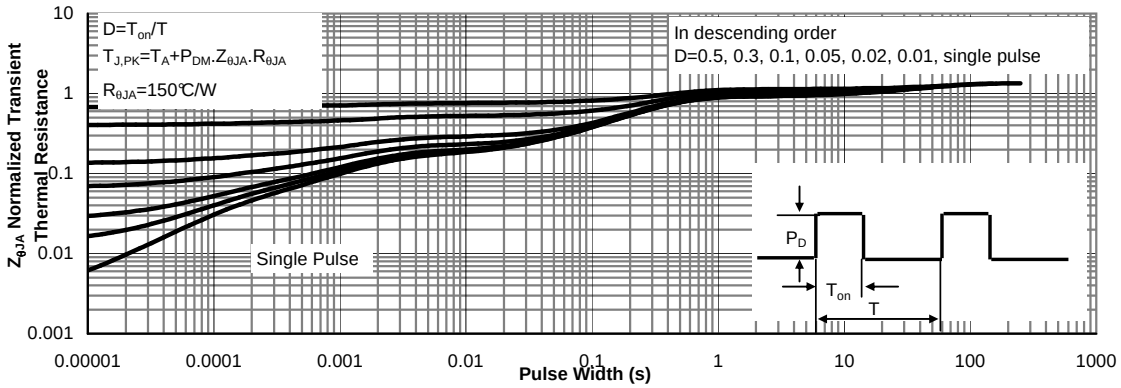


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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