

## General Description

The WSP4099 is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSP4099 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

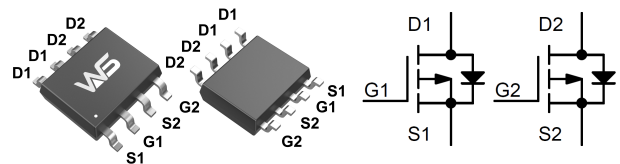
## Product Summary

BVDSS	RDSON	ID
-40V	30mΩ	-6.5A

## Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

## SOP-8 Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-6.5	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-4.5	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-22	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	25	mJ
$I_{AS}$	Avalanche Current	-10	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	2.0	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	110	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	50	$^\circ C/W$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.02	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-6.5A$	---	30	38	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4.5A$	---	46	62	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.5	-2.0	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.72	---	V/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=-32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-4A$	---	8	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-6.5A$	---	7.5	---	nC
$Q_{gs}$	Gate-Source Charge		---	2.4	---	
$Q_{gd}$	Gate-Drain Charge		---	3.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=6\Omega, I_D=-1A, R_L=20\Omega$	---	8.7	---	ns
$T_r$	Rise Time		---	7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	31	---	
$T_f$	Fall Time		---	17	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	668	---	pF
$C_{oss}$	Output Capacitance		---	98	---	
$C_{rss}$	Reverse Transfer Capacitance		---	72	---	

**Guaranteed Avalanche Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	$V_{DD}=-25V, L=0.5\text{mH}, I_{AS}=-10A$	20	---	---	mJ

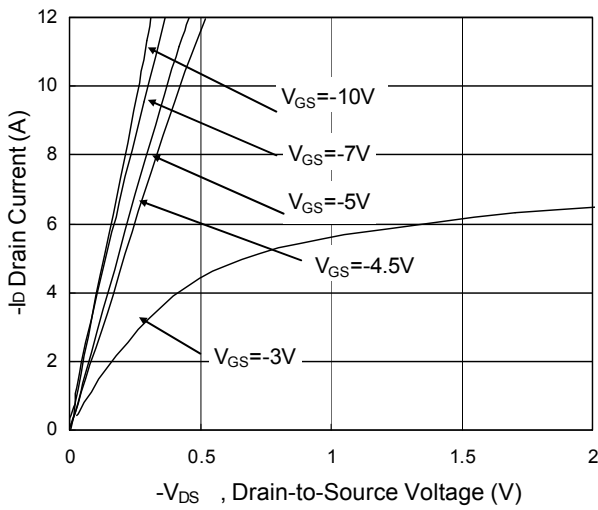
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,6</sup>	$V_G=V_D=0V$ , Force Current	---	---	-2	A
$I_{SM}$	Pulsed Source Current <sup>2,6</sup>		---	---	-22	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.0	V

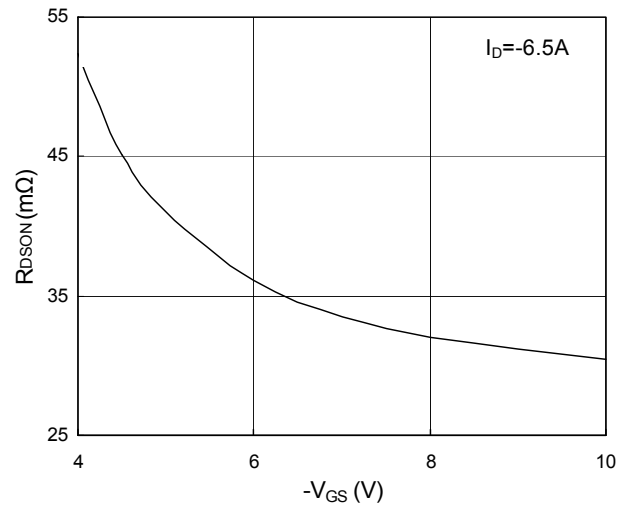
Note :

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper,  $t < 10\text{sec}$ .
- The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$
- The EAS data shows Max. rating. The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.5\text{mH}, I_{AS}=-10A$
- The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

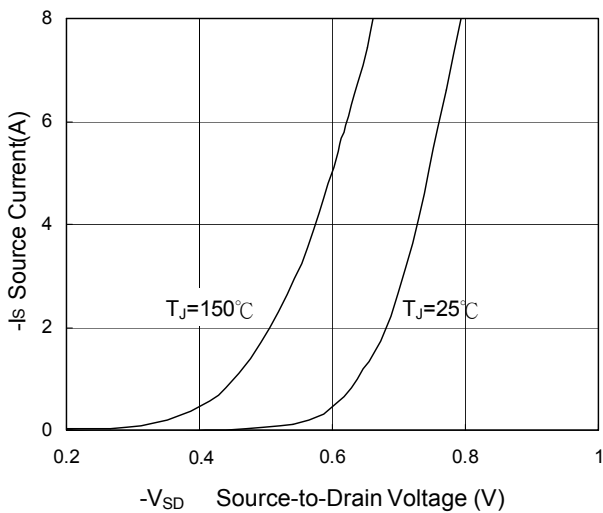
**Typical Characteristics**



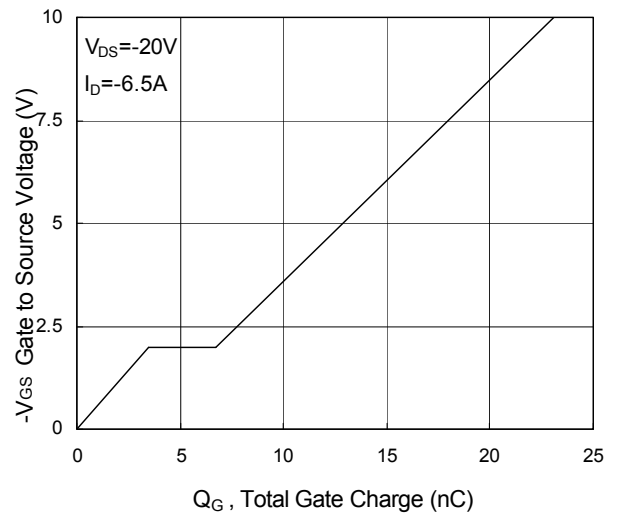
**Fig.1 Typical Output Characteristics**



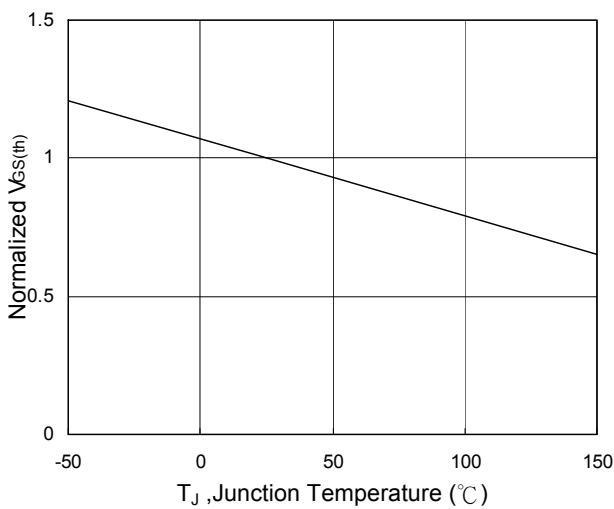
**Fig.2 On-Resistance v.s Gate-Source**



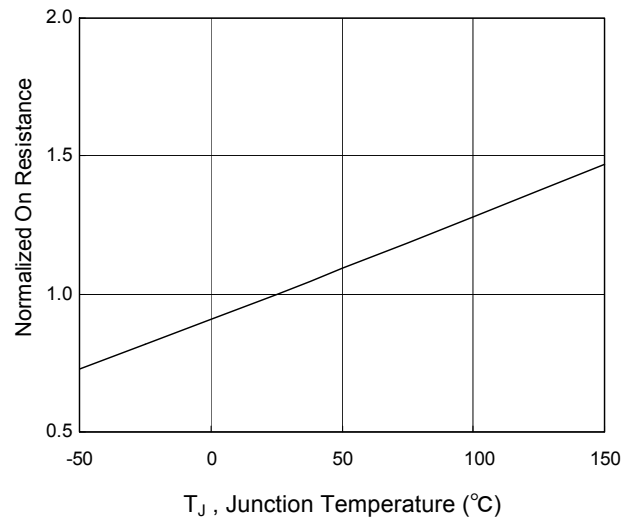
**Fig.3 Forward Characteristics Of Reverse**



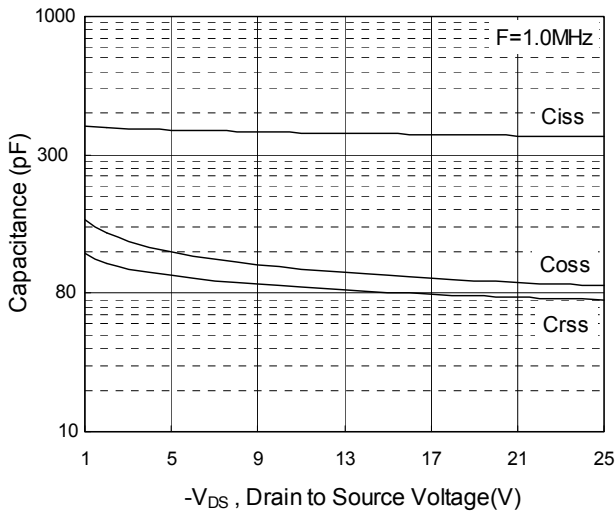
**Fig.4 Gate Charge Characteristics**



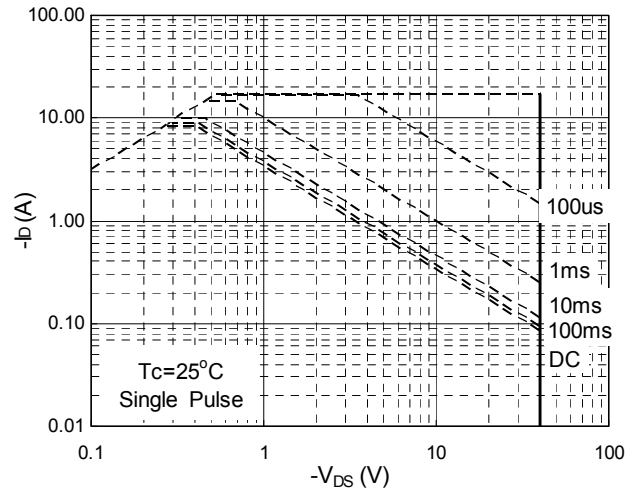
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



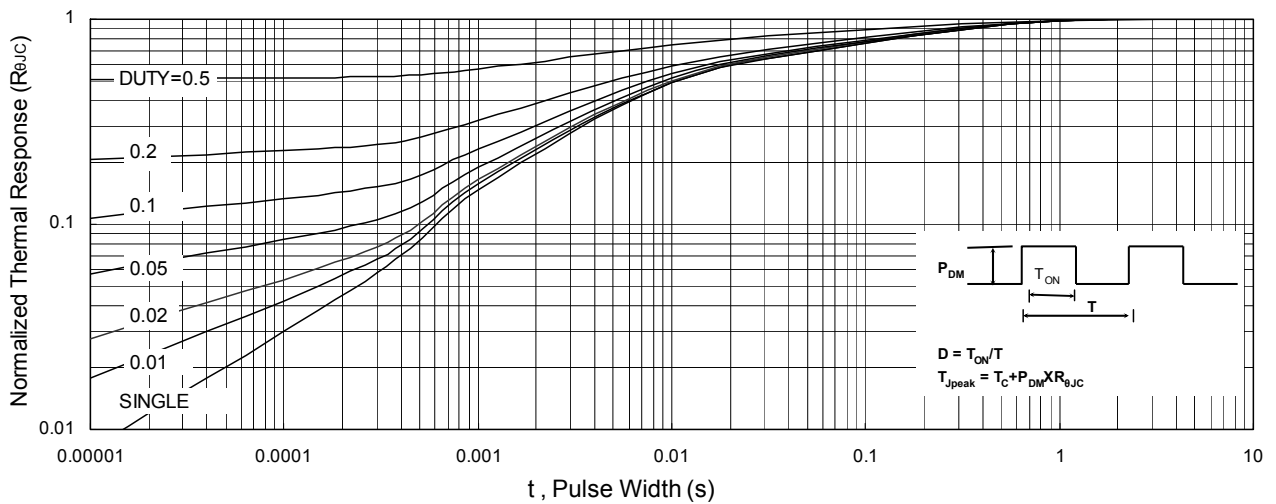
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



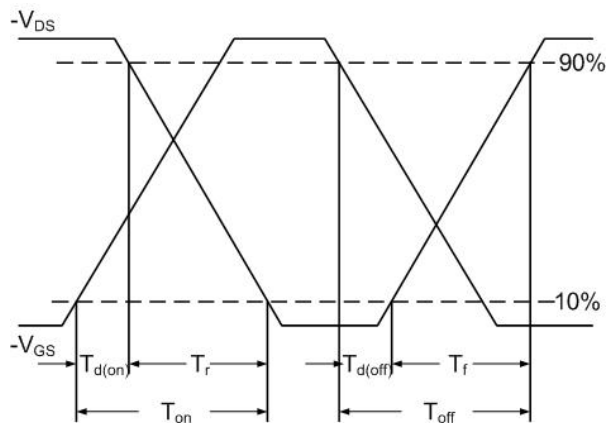
**Fig.7 Capacitance**



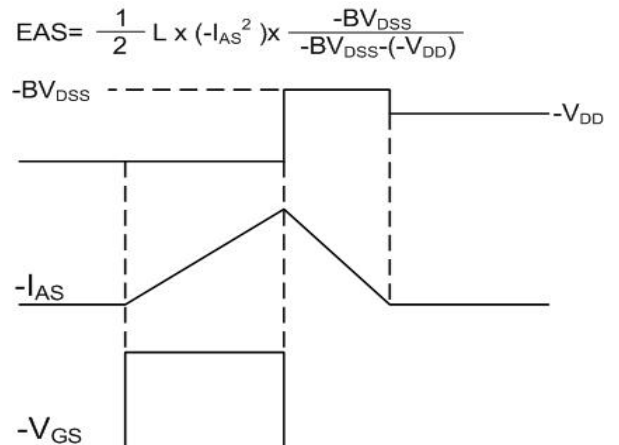
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**



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