TPS748 具有可编程软启动功能的 1.5A 低压降线性稳压器

1 特性

- V_{OUT} 范围：0.8V 至 3.6V
- 超低 V_{IN} 范围：0.8V 至 5.5V
- V_{BIAS} 范围：2.7V 至 5.5V
- 低压降：1.5A、V_{BIAS} = 5V 下的典型值为 60mV
- 电源正常 (PG) 输出可实现电源监视或为其他电源提供时序信号
- 线路、负载和温度范围内的精度为 1%（新芯片）
- 线路、负载和温度范围内的精度为 2%（旧芯片）
- 可编程软启动可提供线性电压启动
- V_{BIAS} 支持低 V_{IN} 运行，具有良好的瞬态响应
- 任何输出电容器 ≥ 2.2 µF 时保持稳定
- 采用小型 3mm × 3mm × 1mm VSON-10 封装和 5mm × 5mm VQFN-20 封装

2 应用

- 网络附加存储 - 企业级
- 机架式服务器
- 网络接口卡 (NIC)
- 商用网络和服务器 PSU

3 说明

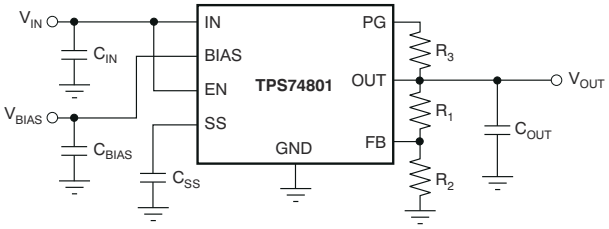
TPS748 低压降 (LDO) 线性稳压器可面向多种应用提供易于使用的稳健型电源管理解决方案。用户可编程软启动通过减少启动时的电容涌入电流，最大限度地减少了输入电源上的应力。软启动具有单调性，旨在为各类处理器和 ASIC 供电。借助使能输入和电源正常输出，可通过外部稳压器轻松实现上电排序。凭借全方位的灵活性，该器件可为 FPGA、DSP 等具有特殊启动要求的应用配置可满足其时序要求的解决方案。

具有精密基准的误差放大器可在整个负载、线路、温度和过程范围内提供 1% 精度（新芯片）。该器件在使用大于或等于 2.2 µF 的任何类型的电容器时都能保持稳定运行，并具有 T_J = –40°C 至 +125°C 的额定结温范围。TPS748 采用小型 3mm × 3mm VSON-10 封装，可实现高度紧凑的解决方案总尺寸。该器件还可采用 5mm × 5mm VQFN-20 封装，从而与 TPS742 兼容。

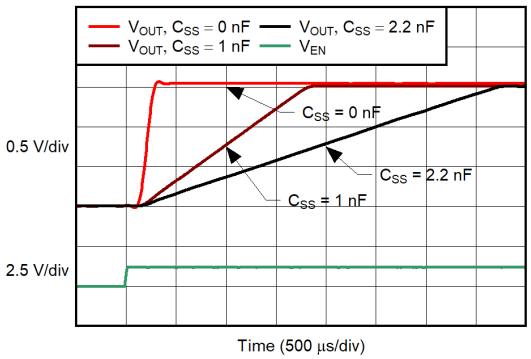
封装信息

器件型号	封装(1)	封装尺寸(2)
TPS748	DRC（VSON，10）	3mm × 3mm
	RGW（VQFN，20）	5mm × 5mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用电路（可调节）



导通响应

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

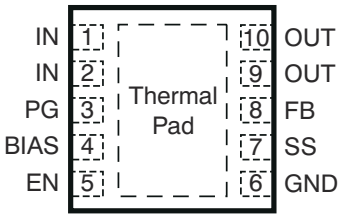

图 4-1. DRC Package, 10-Pin VSON With Thermal Pad (Top View)

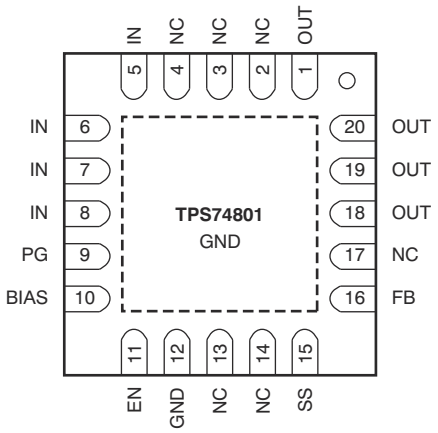

图 4-2. RGW Package, 20-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	VQFN		
BIAS	4	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1-µF or larger input capacitor is recommended for optimal performance. If IN is connected to BIAS, a 4.7-µF or larger capacitor must be used.
EN	5	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
FB	8	16	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	6	12	—	Ground
IN	1, 2	5-8	I	Input to the device. A 1-µF or larger input capacitor is recommended for optimal performance.
NC	N/A	2-4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	9, 10	1, 18-20	O	Regulated output voltage. A small capacitor (total typical capacitance ⩾ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
PG	3	9	O	Power Good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
SS	7	15	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 µs.
Thermal pad			—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power-good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	V_{OUT} + 0.3	5.5	V
V_{EN}	Enable supply voltage		V_{IN}	5.5	V
V_{BIAS} (1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(2)	V_{OUT} + 1.6(2)	5.5	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor(3)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	℃

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

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5.4 Thermal Information

THERMAL METRIC(1)		TPS748				UNIT
		RGW (VQFN)	RGW (VQFN) (2)	DRC (VSON)	DRC (VSON) (2)	
		20 PINS	20 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.6	34.7	44.2	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.3	31.0	50.3	63.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	13.5	19.6	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.4	0.7	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.2	13.5	17.8	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	3.6	4.3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermla metrics application note.
(2) New Chip.

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5.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference (Adj.)	T_A = 25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 1.5 A (Legacy Chip)	–2	±0.5	2	%
		2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 1.5 A (New Chip)	–1	±0.3	1	
ΔV_{OUT} (ΔVIN)	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V (Legacy Chip)		0.03		%/V
		$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V (New Chip)		0.001		
ΔV_{OUT} (ΔIOUT)	Load regulation	50 mA ≤ I_{OUT} ≤ 1.5 A		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V (Legacy Chip) (3)		60	165	mV
		I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V (New Chip) (3)		50	100	
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS} (Legacy Cip)		1.31	1.6	V
		I_{OUT} = 1.5 A, V_{IN} = V_{BIAS} (New Chip)		1.31	1.43	
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2		5.5	A
I_{BIAS}	BIAS pin current	(Legacy Chip)		1	2	mA
		(New Chip)		1	1.2	
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V (Legacy Chip)		1	50	µA
		V_{EN} ≤ 0.4 V (New Chip)		0.85	2.75	
I_{FB}	Feedback pin current	(Legacy Chip)	–1	0.15	1	µA
		(New Chip)	–30	0.15	30	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		60		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (Legacy Chip)		50		
		1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (New Chip)		59		
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (Legacy Chip)		30		
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (New Chip)		50		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 1 nF (Legacy Chip)		25 × V_{OUT}		µVrms
		BW = 100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 1 nF (New Chip)		20 × V_{OUT}		
t_{STR}	Minimum startup time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open (Legacy Chip)		200		µs
		R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open (New Chip)		250		
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V (Legacy Chip)		440		nA
		V_{SS} = 0.4 V (New Chip)		530		
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis	(Legacy Chip)		50		mV
		(New Chip)		55		
$V_{EN(dg)}$	Enable pin deglitch time			20		µs

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5.5 Electrical Characteristics（续）

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 μF, C_{IN} = C_{OUT} = 10 μF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Enable pin current	V_{EN} = 5 V (Legacy Chip)		0.1	1	μA
		V_{EN} = 5 V (New Chip)		0.1	0.3	
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT} (Legacy Chip)			0.3	V
		I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT} (New Chip)			0.125	
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT} (Legacy Chip)		0.1	1	μA
		V_{PG} = 5.25 V, V_{OUT} > V_{IT} (New Chip)		0.001	0.05	
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		
$R_{PULLDOWN}$	Output pulldown resitance	V_{BIAS} = 5V, V_{EN} = 0V		0.83	1	kΩ

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 5-11.

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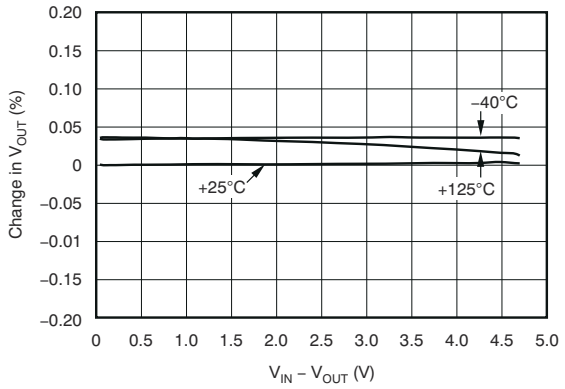
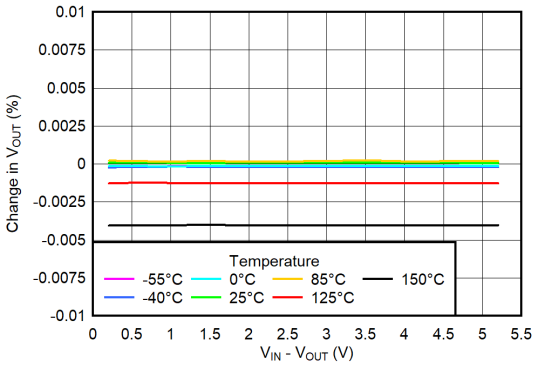
5.6 Typical Characteristics: I_{OUT} = 50 mA

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



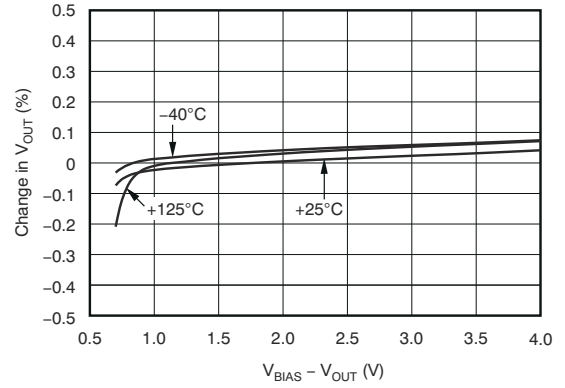
Legacy chip

图 5-1. V_{IN} Line Regulation



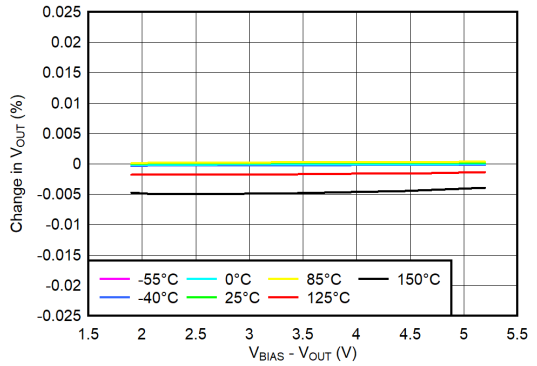
New chip

图 5-2. V_{IN} Line Regulation



Legacy chip

图 5-3. V_{BIAS} Line Regulation



New chip

图 5-4. V_{BIAS} Line Regulation

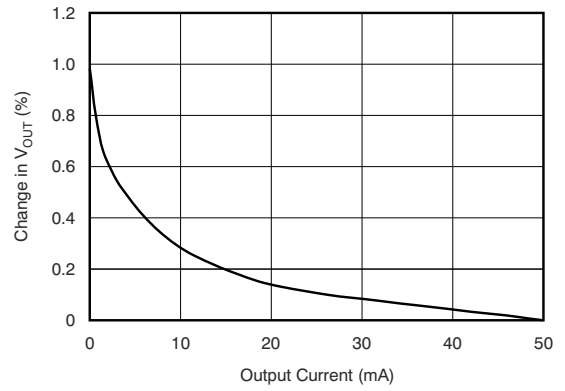
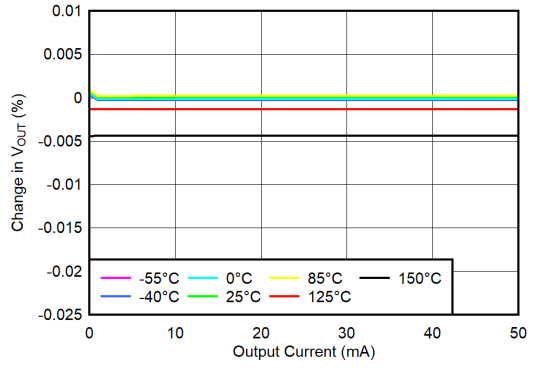


图 5-5. Load Regulation at Light Load



New chip

图 5-6. Load Regulation at Light Load

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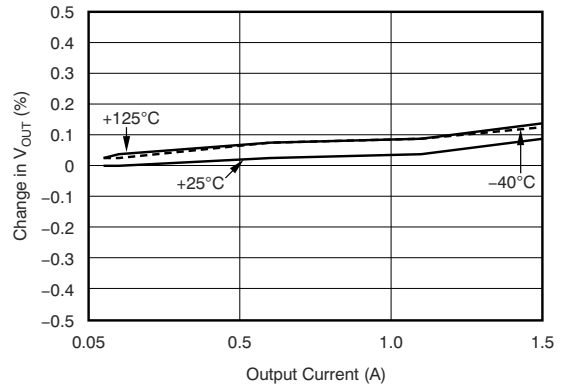
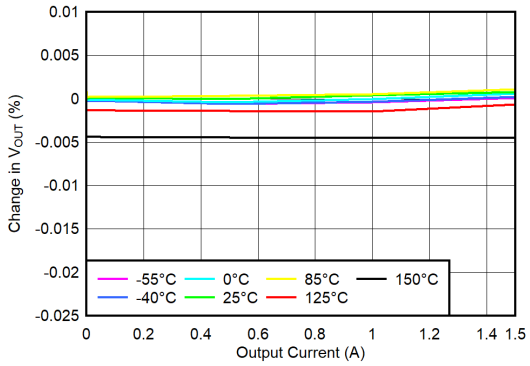
5.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



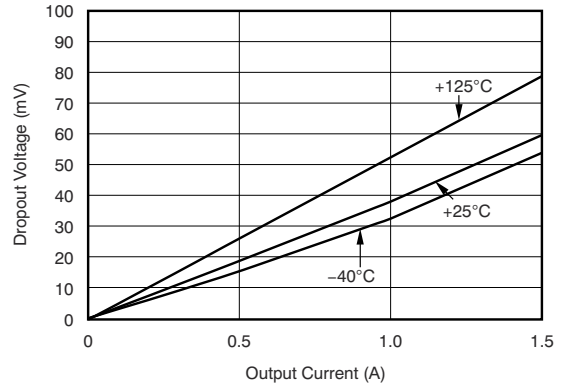
Legacy chip

图 5-7. Load Regulation



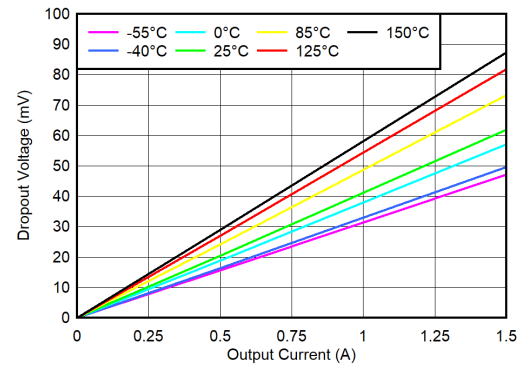
New chip

图 5-8. Load Regulation



Legacy chip

图 5-9. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)



New chip

图 5-10. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

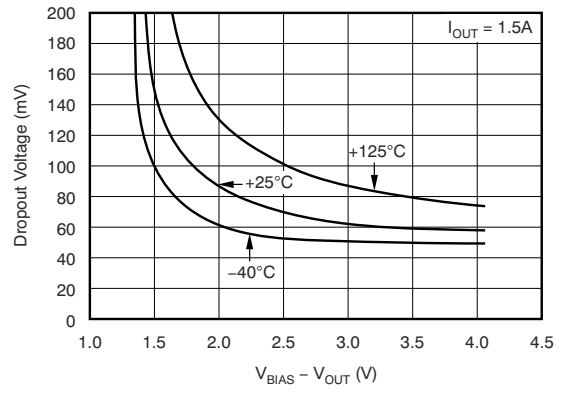


图 5-11. V_{IN} Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

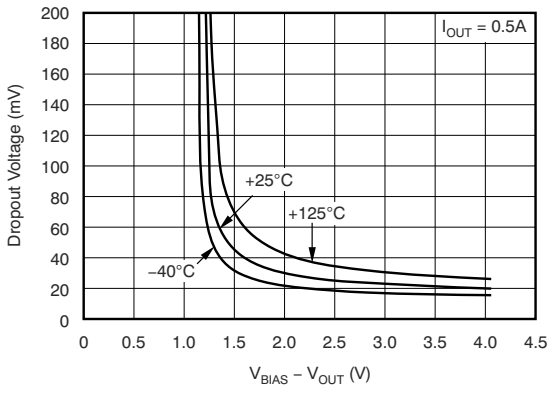


图 5-12. V_{IN} Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

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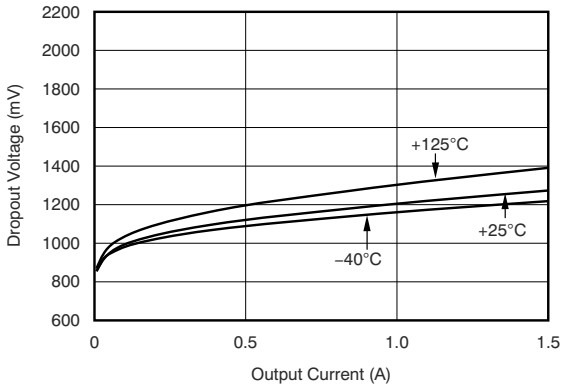
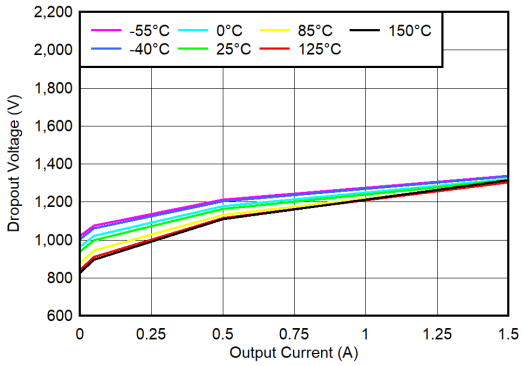
5.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



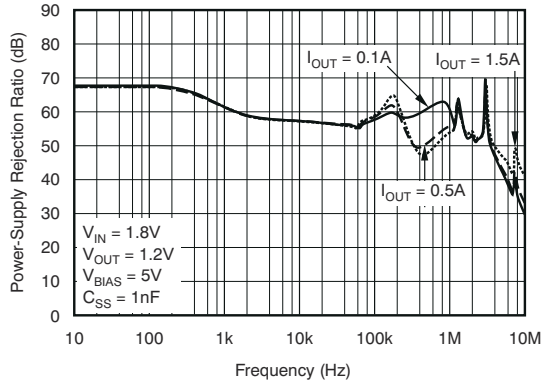
Legacy chip

图 5-13. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)



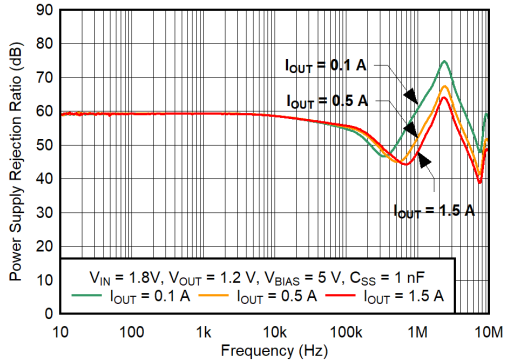
New chip

图 5-14. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)



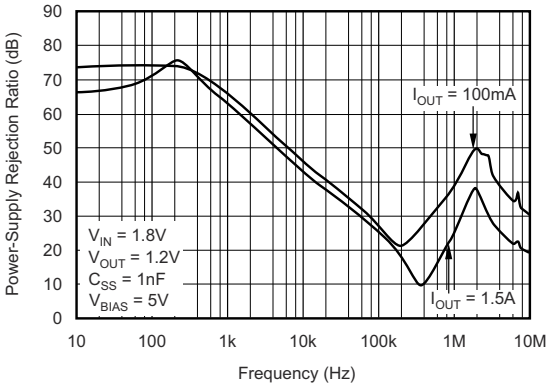
Legacy chip

图 5-15. V_{BIAS} PSRR vs Frequency



New chip

图 5-16. V_{BIAS} PSRR vs Frequency



Legacy chip

图 5-17. V_{IN} PSRR vs Frequency

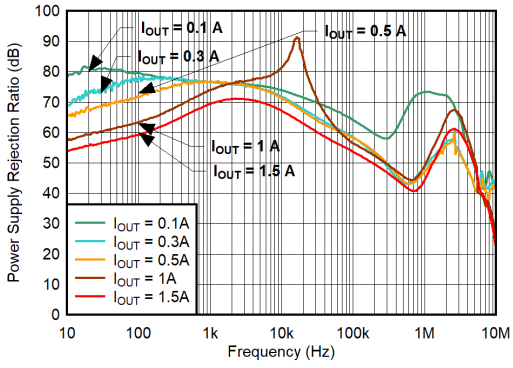


图 5-18. V_{IN} PSRR vs Frequency

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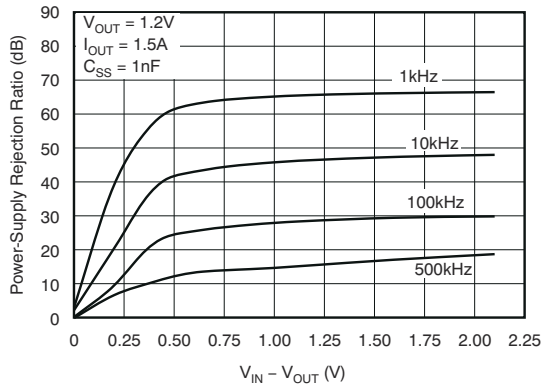
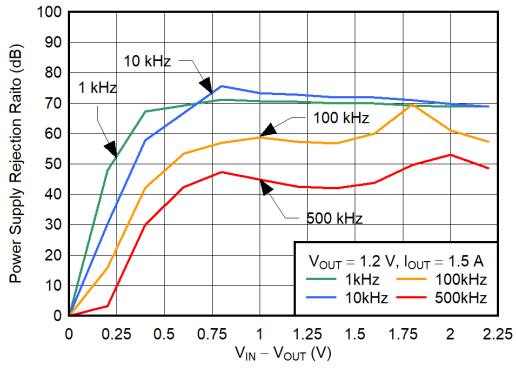
5.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



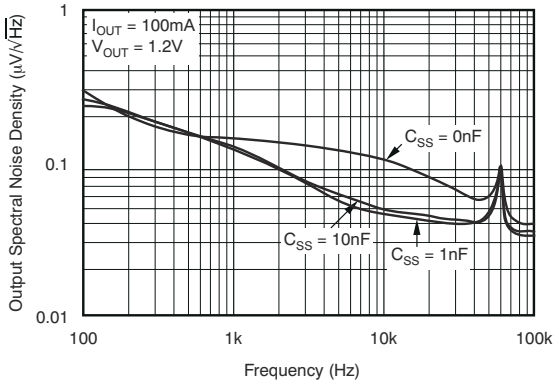
Legacy chip

图 5-19. V_{IN} PSRR vs (V_{IN} – V_{OUT})



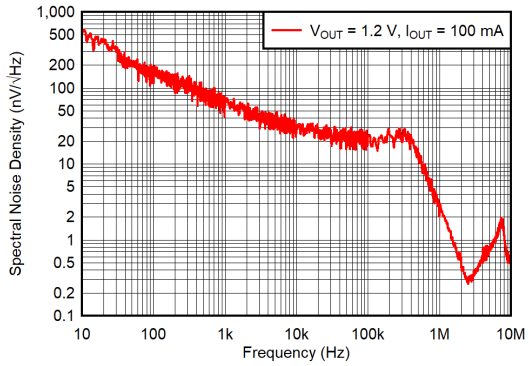
New chip

图 5-20. V_{IN} PSRR vs (V_{IN} – V_{OUT})



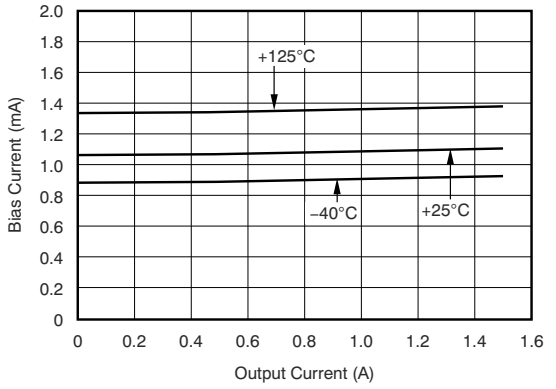
Legacy chip

图 5-21. Noise Spectral Density



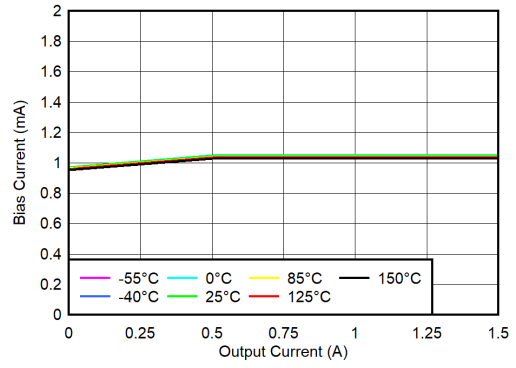
New chip

图 5-22. Noise Spectral Density



Legacy chip

图 5-23. BIAS Pin Current vs Output Current and Temperature (T_J)



New chip

图 5-24. BIAS Pin Current vs Output Current and Temperature (T_J)

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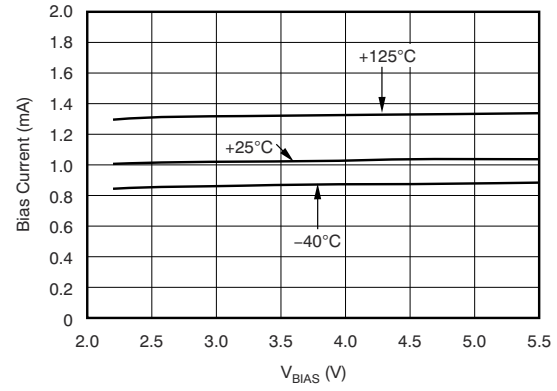
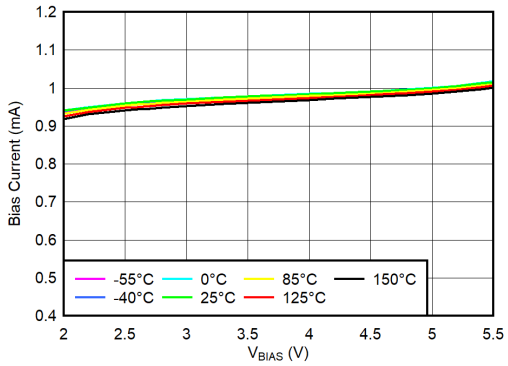
5.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



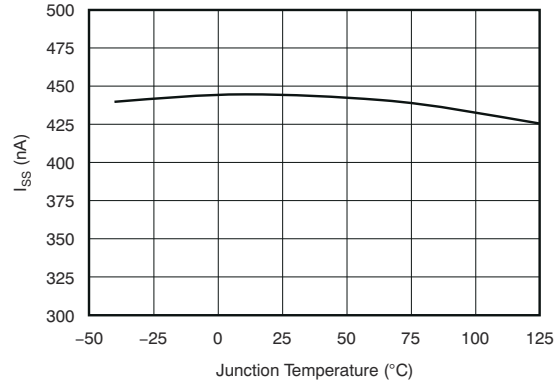
Legacy chip

图 5-25. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)



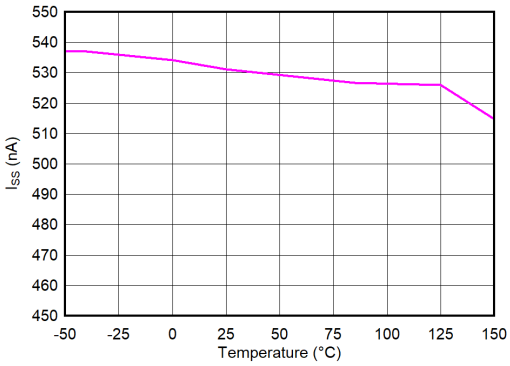
New chip

图 5-26. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)



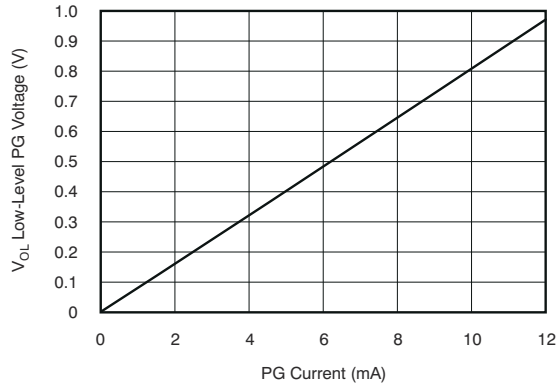
Legacy chip

图 5-27. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)



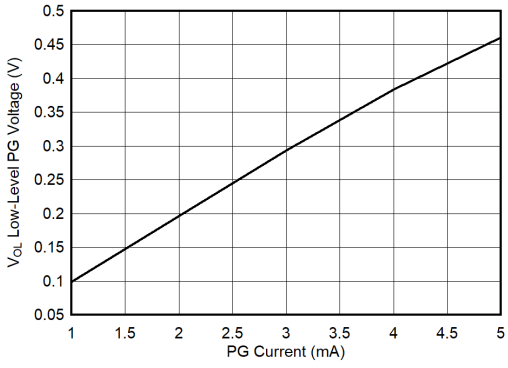
New chip

图 5-28. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)



Legacy chip

图 5-29. Low-Level PG Voltage vs Current



New chip

图 5-30. Low-Level PG Voltage vs Current

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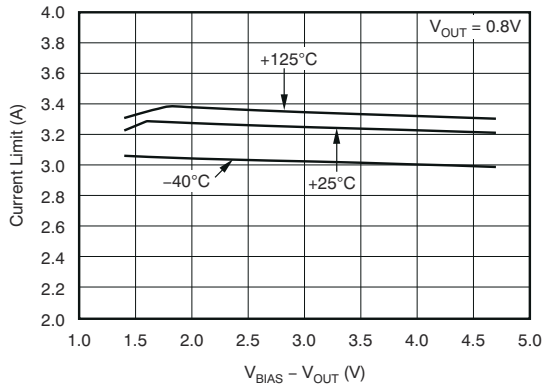
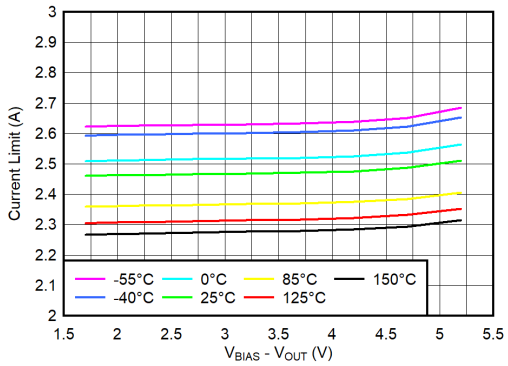
5.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 4.7 μF, and C_{OUT} = 10 μF (unless otherwise noted)



Legacy chip

图 5-31. Current Limit vs (V_{BIAS} – V_{OUT})

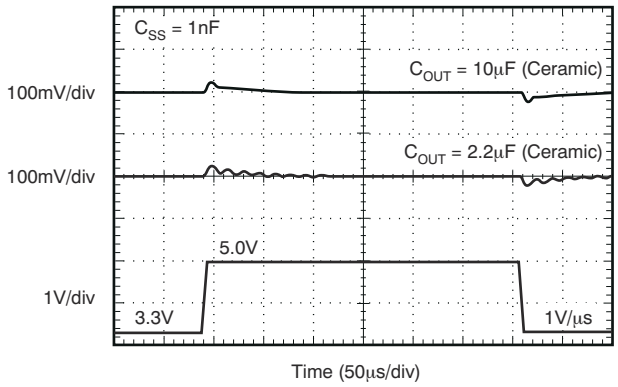


New chip

图 5-32. Current Limit vs (V_{BIAS} – V_{OUT})

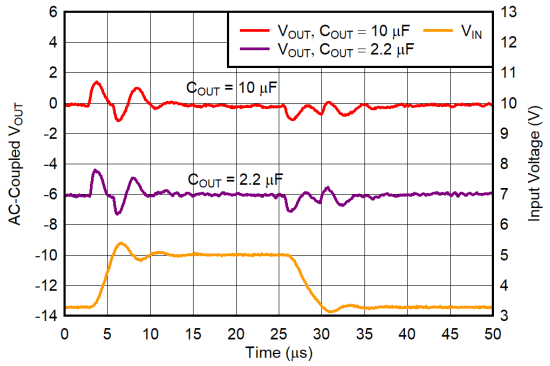
5.7 Typical Characteristics: I_{OUT} = 1 A

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



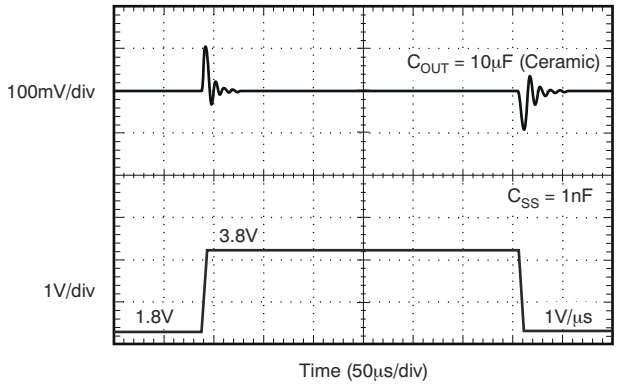
Legacy chip

图 5-33. V_{BIAS} Line Transient



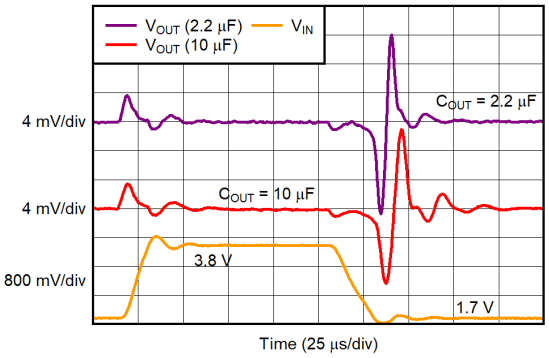
New chip

图 5-34. V_{BIAS} Line Transient



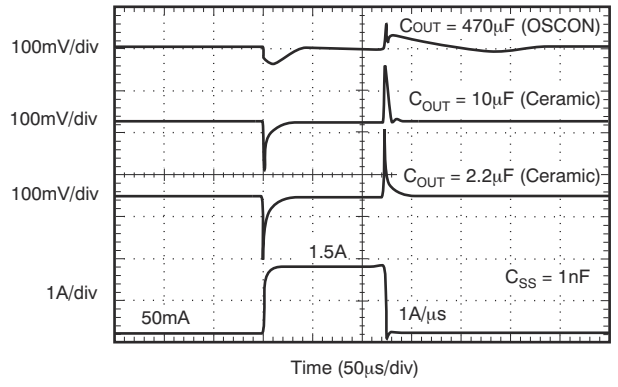
Legacy chip

图 5-35. V_{IN} Line Transient



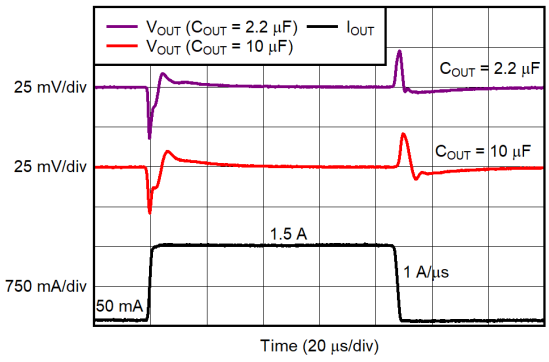
New chip

图 5-36. V_{IN} Line Transient



Legacy chip

图 5-37. Output Load Transient Response



New chip

图 5-38. Output Load Transient Response

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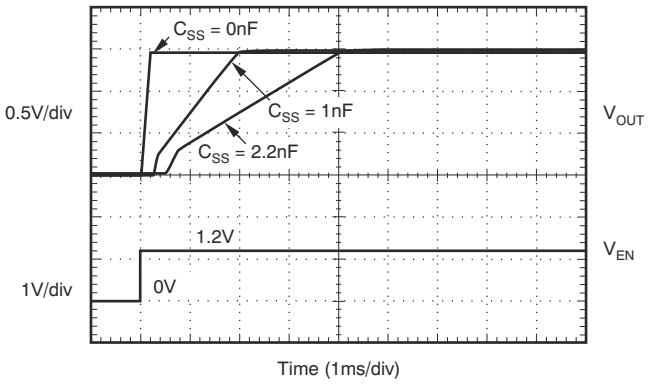
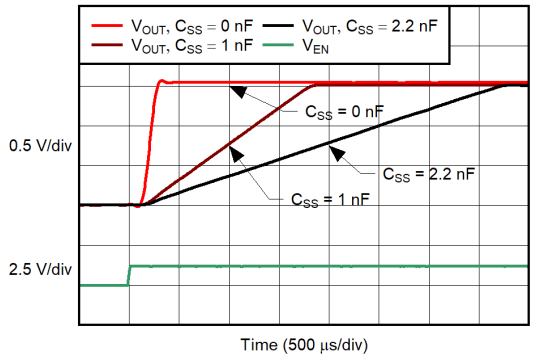
5.7 Typical Characteristics: I_{OUT} = 1 A (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



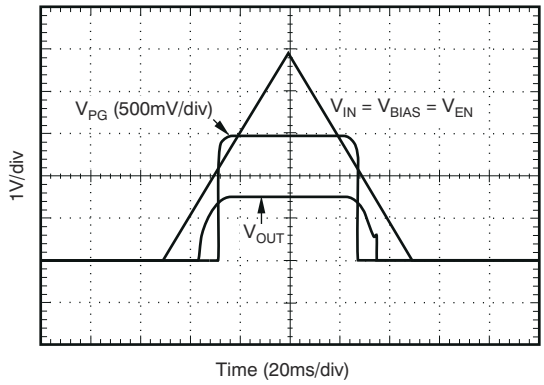
Legacy chip

图 5-39. Turn-On Response



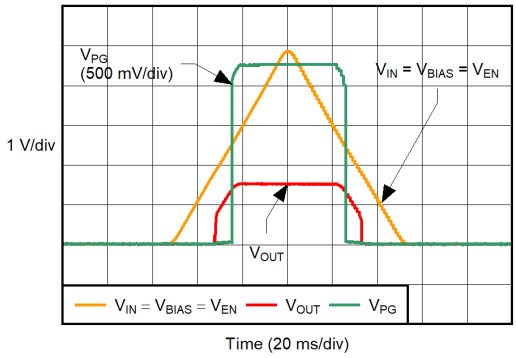
New chip

图 5-40. Turn-On Response



Legacy chip

图 5-41. Power-Up, Power-Down



New chip

图 5-42. Power-Up, Power-Down

6 Detailed Description

6.1 Overview

The TPS748 is a low-dropout regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS748 to be stable with any capacitor type of value 2.2 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS748 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

6.2 Functional Block Diagrams

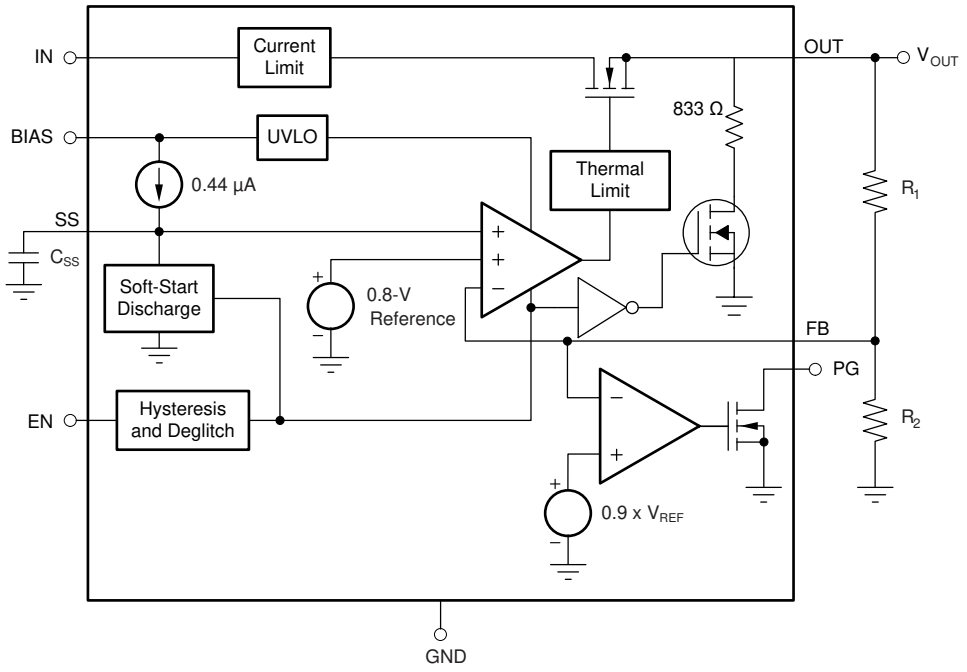


图 6-1. Legacy Chip Functional Block Diagram

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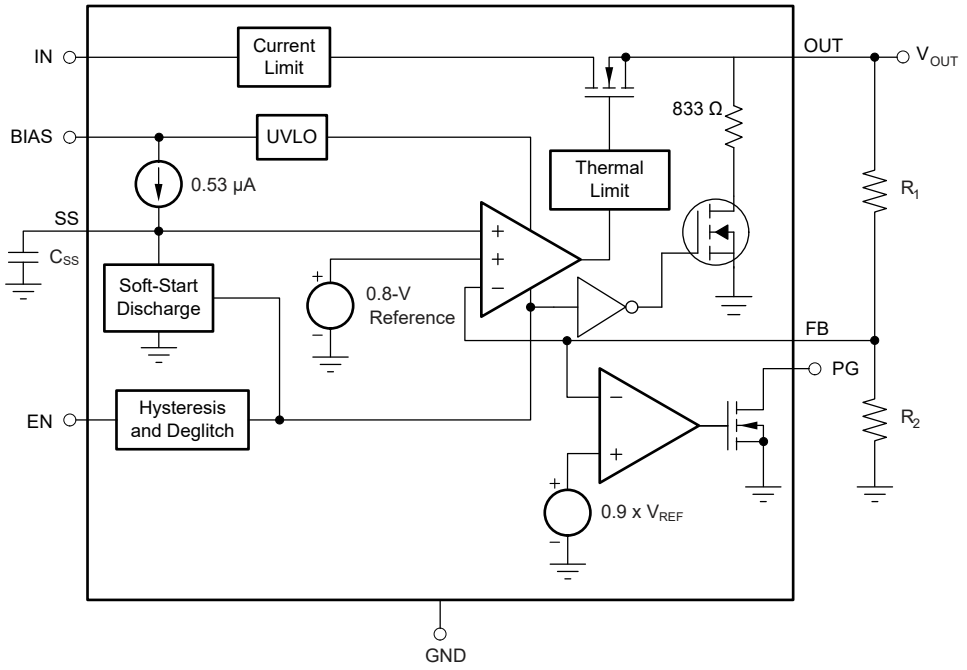

图 6-2. New Chip Functional Block Diagram

6.3 Feature Description

6.3.1 Enable/Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS748 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS748.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, connect this pin as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

The TPS748 has an internal active pulldown circuit that connects the output to GND through an 833-Ω resistor when the device is disabled. This resistor discharges the output with a time constant of:

$$\tau = \left(\frac{833 \times R_L}{833 + R_L} \right) \times C_{OUT} \tag{1}$$

6.3.2 Power Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

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6.3.3 Internal Current Limit

The TPS748 features a factory-trimmed current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 2 A and maintain regulation. The current limit responds in approximately 10 μs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS748 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS748 above the rated current degrades device reliability.

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heat sinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS748 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS748 into thermal shutdown degrades device reliability.

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6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geqslant V_{OUT} + 1.6$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.6$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 165°C$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass transistor is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

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6.5 Programming

6.5.1 Programmable Soft-Start

The TPS74801 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because soft-start eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74801 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using 方程式 2:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \tag{2}$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor can set the start-up time. In this case, the start-up time is given by 方程式 3:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \tag{3}$$

where:

- $V_{OUT(nom)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(min)}$ is the minimum current limit for the device

In applications where monotonic start up is required, the soft-start time given by 方程式 2 must be set greater than 方程式 3.

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit can possibly be unable to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF can be a problem in applications where the enable pin must be rapidly pulsed and with the device still required to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See 表 6-2 for suggested soft-start capacitor values.

表 6-2. Standard Capacitor Values for Programming the Soft-Start Time

C_{SS}	SOFT-START TIME(1) (Legacy Chip)	SOFT-START TIME(1) (New Chip)
Open	0.1 ms	0.25ms
270 pF	0.5 ms	0.4ms
560 pF	1 ms	0.8ms
2.7 nF	5 ms	4.1ms
5.6 nF	10 ms	8.5ms
10 nF	18 ms	15ms

(1) $t_{SS}(s) = 0.8 \times C_{SS}(F) / I_{SS}$, where $t_{SS}(s)$ = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor; see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note for more information.

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6.5.2 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until reaching the set output voltage
- If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}
- If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}
- If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor

图 6-3 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

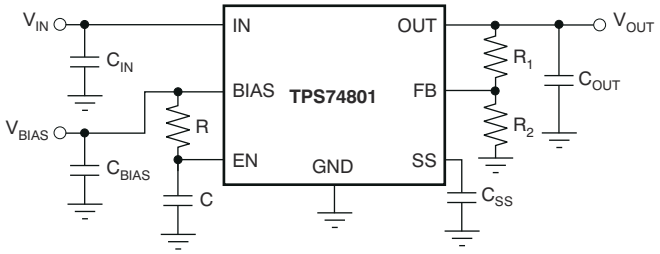


图 6-3. Soft-Start Delay Using an RC Circuit to Enable the Device

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

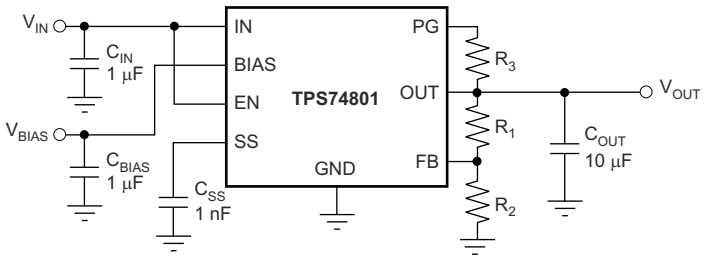
The TPS748 is a low-dropout regulator that features soft-start capability. This regulator uses a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS748 to be stable with any capacitor type of value 2.2 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS748 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.1.1 Adjusting the Output Voltage

图 7-1 shows the typical application circuit for the TPS748 adjustable output device.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

图 7-1. Typical Application Circuit for the TPS748 (Adjustable)

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R_1 and R_2 can be calculated for any output voltage using the formula shown in 图 7-1. 表 7-1 lists sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 must be ⩽ 4.99 kΩ.

表 7-1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$.

备注

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 μA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

7.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors ⩾ 2.2 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 μF and minimum recommended capacitor for V_{BIAS} is 0.1 μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF. Use good-quality, low-ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance.

7.1.3 Transient Response

The TPS748 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance does. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see 图 5-37 in the *Typical Characteristics* section. Because the TPS748 is stable with output capacitors as low as 2.2 μF, many applications can then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

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7.1.4 Dropout Voltage

The TPS748 offers very low dropout performance, making the device designed for high-current, low V_{IN}, low V_{OUT} applications. The low dropout of the TPS748 allows the device to be used in place of a dc/dc converter and still achieve good efficiency. 方程式 4 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{4}$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

There are two different specifications for dropout voltage with the TPS748. The first specification (see 图 7-2) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 3.25 V[1] above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} +3.25 V[1], V_{IN} dropout is less than specified.[1]

The second specification (illustrated in 图 7-8) is referred to as *V_{BIAS} dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.6 V above V_{OUT}. Because of this usage, IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

7.1.5 Output Noise

The TPS748 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF soft-start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 1-nF soft-start capacitor is given in 方程式 5:

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{5}$$

The low output noise of the TPS748 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

[1] 3.25 V is a test condition of this device and can be adjusted by referring to 图 5-11.

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7.2 Typical Applications

7.2.1 FPGA I/O Supply at 1.5 V With a Bias Rail

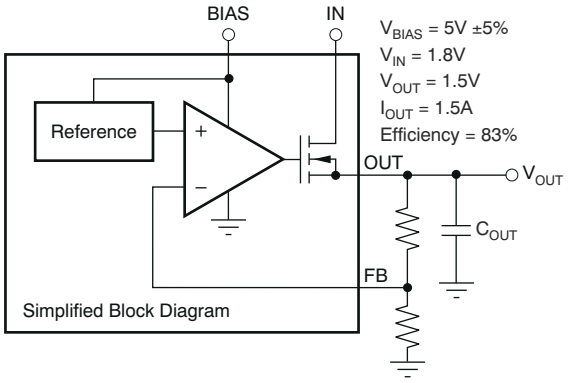

图 7-2. Typical Application of the TPS748 Using an Auxiliary Bias Rail

7.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA , at $V_{OUT(nom)}$ = 1.5 V and $I_{OUT(dc)}$ = 1.5 A. The available external supply voltages are 1.8 V, 3.3 V, and 5 V.

7.2.1.2 Detailed Design Procedure

First, determine what supplies to use for the input and bias rails. A 1.8-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 165 mV if V_{BIAS} is at least 3.25 V higher than V_{OUT}. To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in 方程式 4 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As 表 7-1 describes, set R_1 = 4.12 kΩ and R_2= 4.75 kΩ to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; see the *Input, Output, and Bias Capacitor Requirements* section for C_{IN} = 1 µF, C_{BIAS} = 1 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 1.8-ms start-up time.

图 7-2 shows a simplified version of the final circuit.

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7.2.1.3 Application Curves

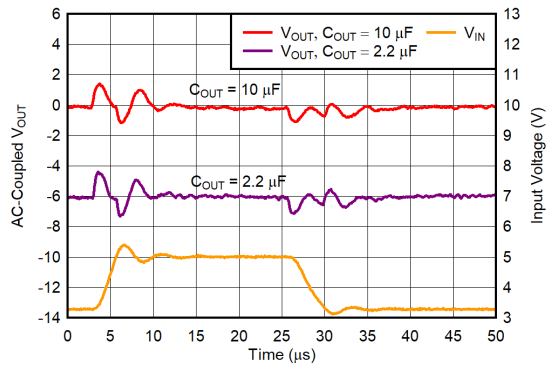

图 7-3. V_{BIAS} Line Transient

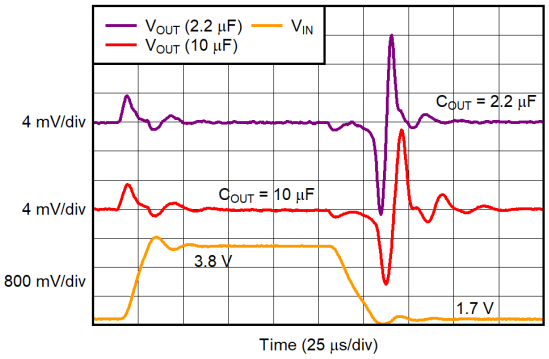

图 7-4. V_{IN} Line Transient

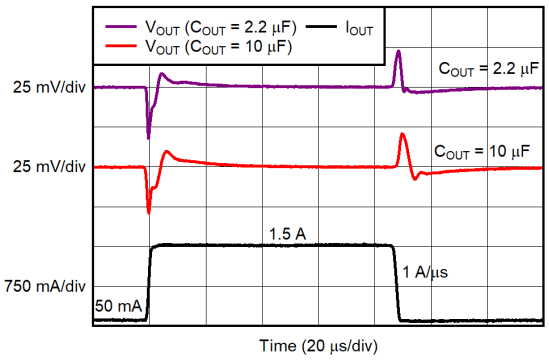

图 7-5. Output Load Transient Response

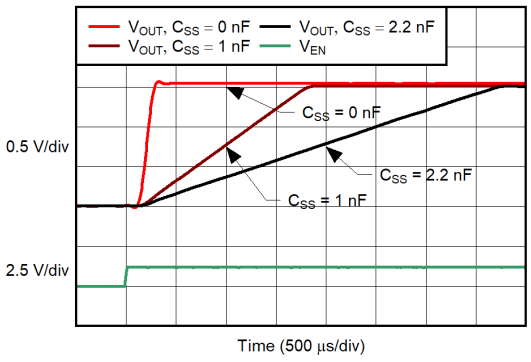

图 7-6. Turn-On Response

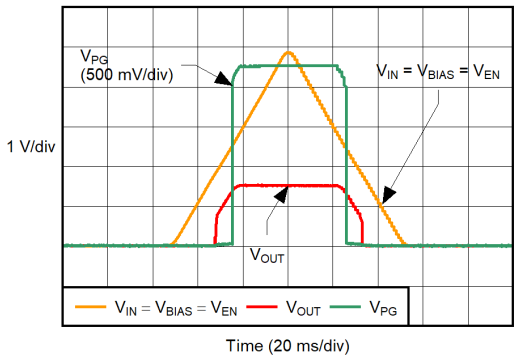

图 7-7. Power-Up, Power-Down

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7.2.2 FPGA I/O Supply at 1.5 V Without a Bias Rail

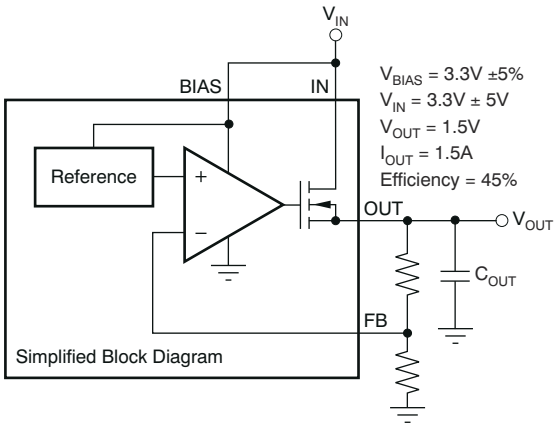

图 7-8. Typical Application of the TPS748 Without an Auxiliary Bias Rail

7.2.2.1 Design Requirements

The application powers the I/O rails of an FPGA, at $V_{OUT(nom)}$ = 1.5 V and $I_{OUT(max)}$ = 1.5 A. The only available rail is 3.3 V. The I/O pins are driven for only short durations with a 5% duty cycle, so thermal issues are not a concern.

7.2.2.2 Detailed Design Procedure

There is only one available rail; therefore, the input supply and the bias supply are connected together on the 3.3-V input supply.

The output voltage must be set to 1.5 V. As 表 7-1 describes, set R_1 = 4.12 kΩ and R_2 = 4.75 kΩ to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; see the *Input, Output, and Bias Capacitor Requirements* section for C_{IN} = C_{BIAS} = 4.7 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 1.8-ms start-up time.

图 7-8 shows the TPS748 configured without a bias rail.

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7.2.2.3 Application Curves

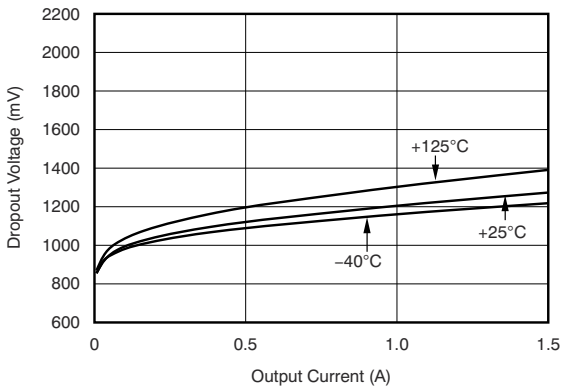

图 7-9. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

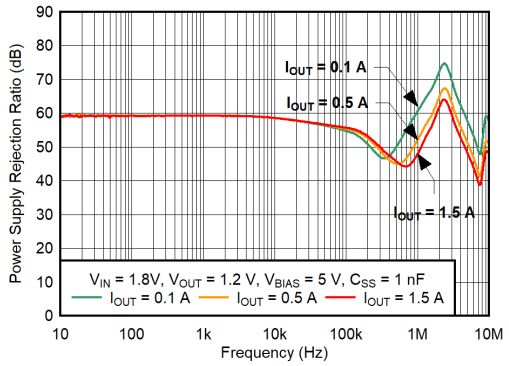

图 7-10. V_{BIAS} PSRR vs Frequency

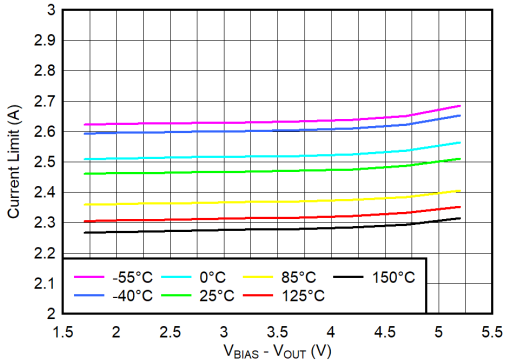

图 7-11. Current Limit vs (V_{BIAS} – V_{OUT})

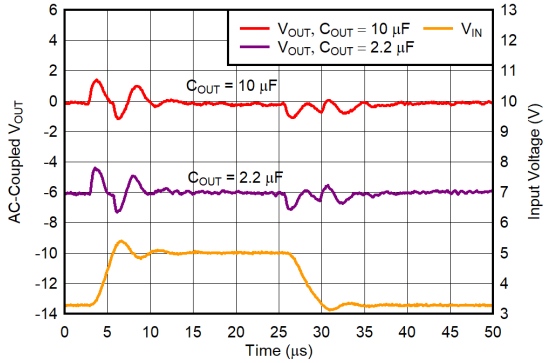

图 7-12. V_{BIAS} Line Transient

7.3 Power Supply Recommendations

The TPS748 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.62 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin of the TPS748. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in 图 7-1 must be connected as close as possible to the load. If BIAS is connected to IN, connect

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BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using 方程式 6:

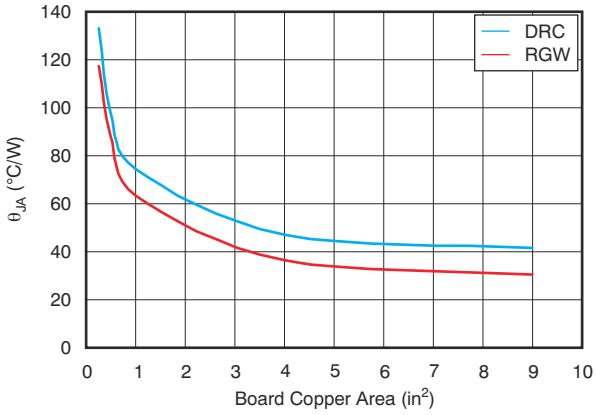
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both the VSON (DRC) and VQFN (RGW) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using 方程式 7:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (7)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using 图 7-13.



$R_{\theta JA}$ value at board size of 9 in^2 (that is, 3 in × 3i n) is a JEDEC standard.

图 7-13. $R_{\theta JA}$ vs Board Size

图 7-13 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

备注

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

7.4.1.1 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 方程式 8). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

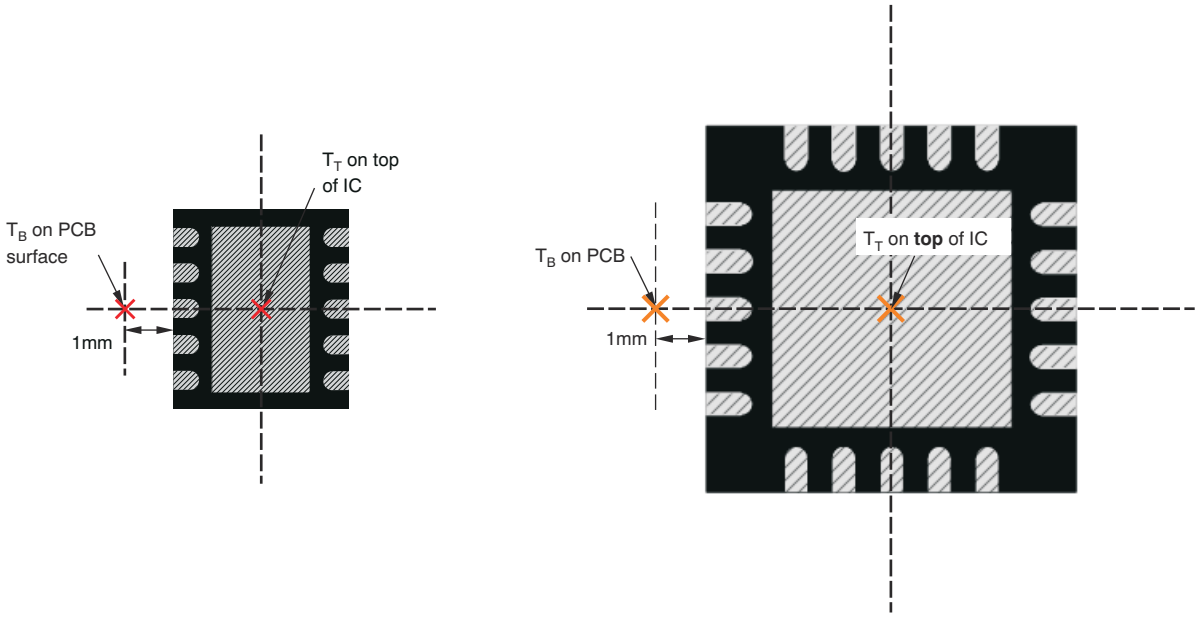
$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{8}$$

Where P_D is the power dissipation shown by 方程式 6, T_T is the temperature at the center-top of the device package, and T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface* (图 7-14).

备注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.



(a) Example DRC (SON) Package Measurement (b) Example RGW (QFN) Package Measurement

图 7-14. Measuring Points for T_T and T_B

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By looking at 图 7-15, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with 方程式 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

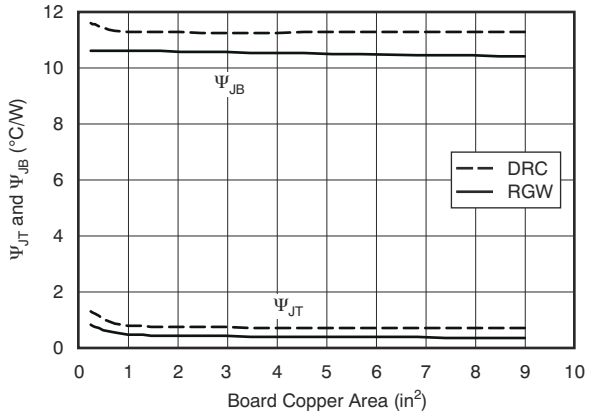

图 7-15. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *IC Package Thermal Metrics* application note, also available on the TI website.

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7.4.2 Layout Example

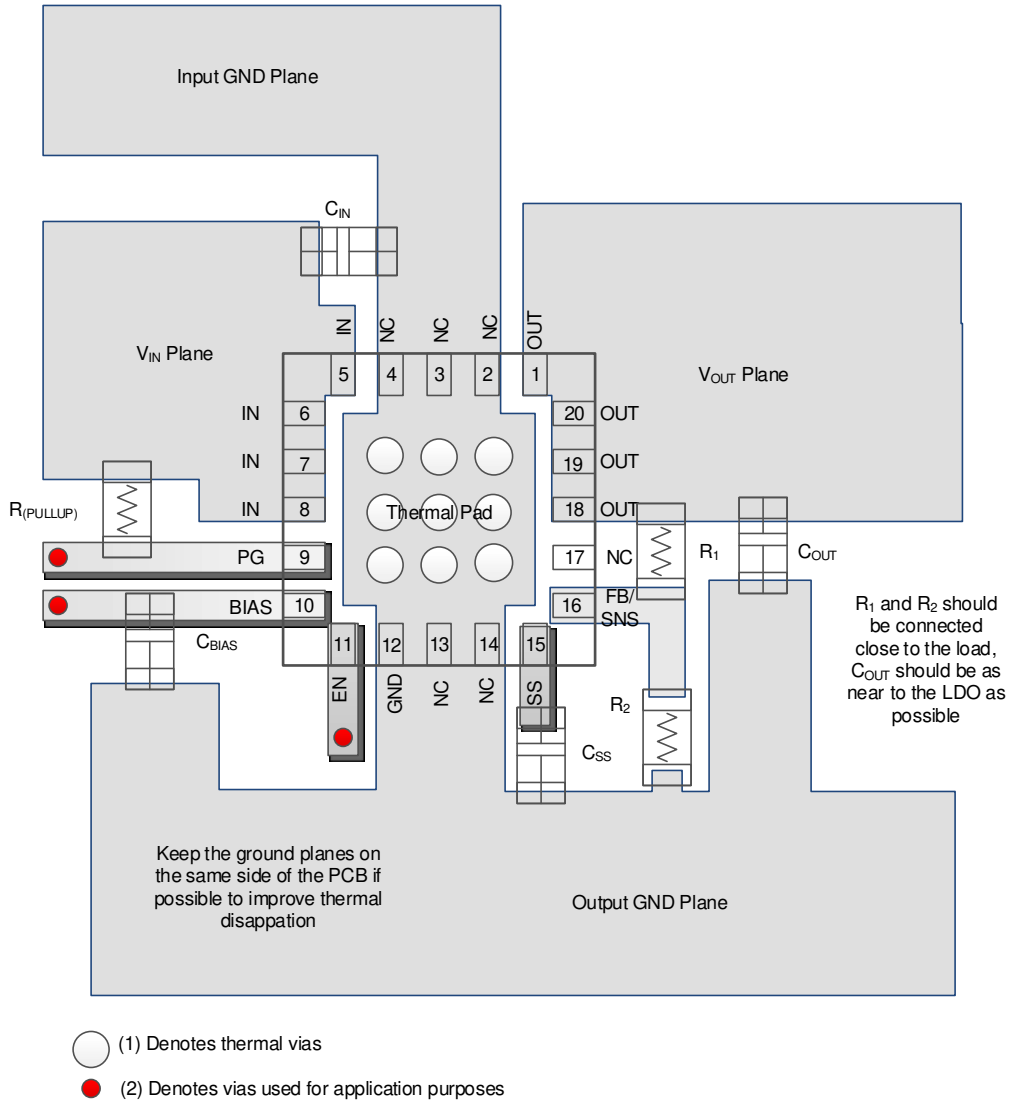

图 7-16. Layout Example (RGW Package)

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS74801**yyyzM3**	**yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. The device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.1.2 Development Support

8.1.2.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS48. The TPS74801EVM-177 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.2.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS748 is available through the product folders under *Tools & Software*.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Ultimate Regulation with Fixed Output Versions of TPS742xx, TPS743xx, and TPS744xx* application note
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *TPS74701EVM-177 and TPS74801EVM-177* user's guide

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

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8.6 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (April 2023) to Revision N (June 2024)	Page
• 将 M3 引用更改为*新芯片*	1
• 将*说明* 部分中的 *2% 精度* 更改为 *1% 精度 (新芯片)*	1
• Added new chip plots to *Typical Characteristics* sections	8
• Added *New Chip Functional Block Diagram* to *Functional Block Diagrams* section	16
• Changed *Standard Capacitor Values for Programming the Soft-Start Time* table: corrected equation in footnote and added *soft-start time* column for new chip	20
• Changed both *Application Curves* sections in *Typical Applications* to use new chip curves	26
• Added *Device Nomenclature* section	33

Changes from Revision L (March 2017) to Revision M (April 2023)	Page
• *更新了整个文档中的表格、图和交叉参考的编号格式*	1
• 通篇将 QFN 更改为 VQFN	1
• 向文档中添加了 M3 器件、M3 *专有电气特性* 表和*典型特性* 部分	1
• 添加了指向*应用* 部分的链接	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74801DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCRM3	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCRM3.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801DRCTG4	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO
TPS74801RGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWRG4	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWRM3	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWRM3.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801
TPS74801RGWTG4	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS74801 :

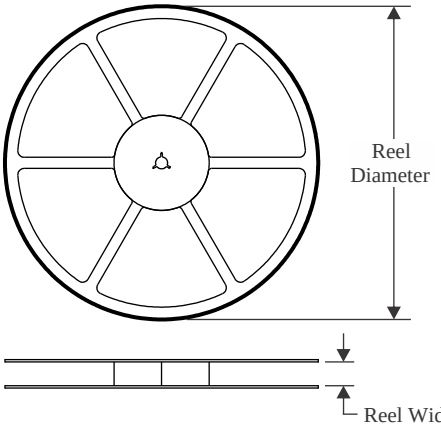
- Automotive : TPS74801-Q1

NOTE: Qualified Version Definitions:

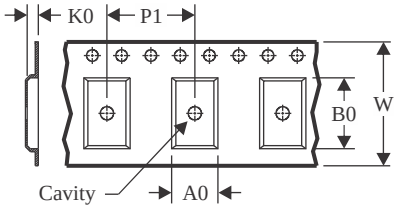
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

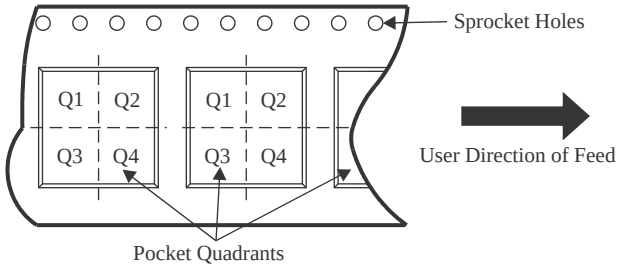


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

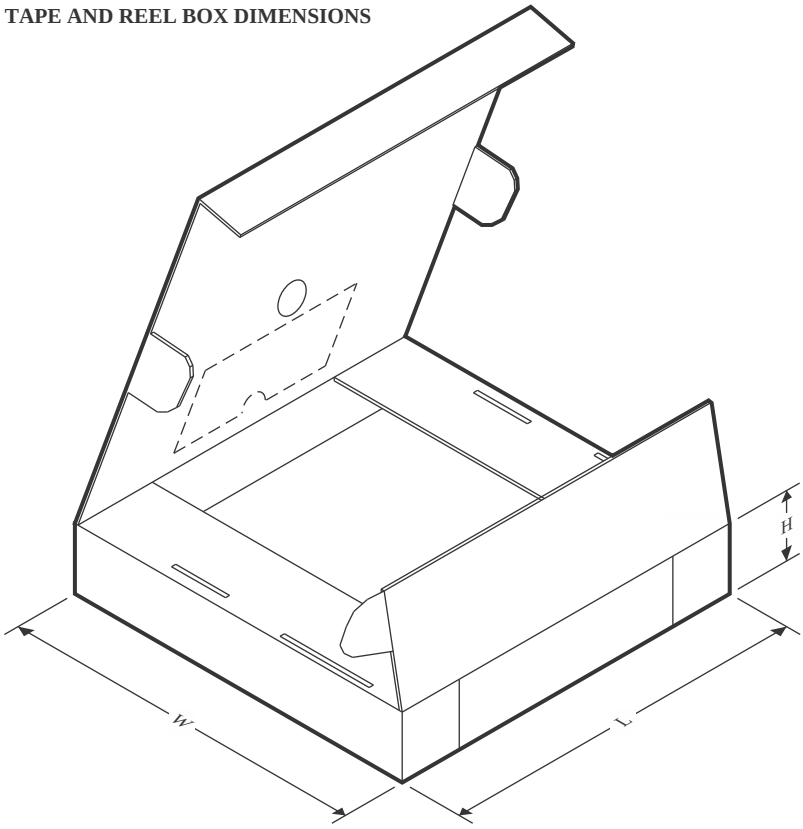
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCRM3	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74801RGWRM3	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74801RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801DRCRM3	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74801RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWRM3	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

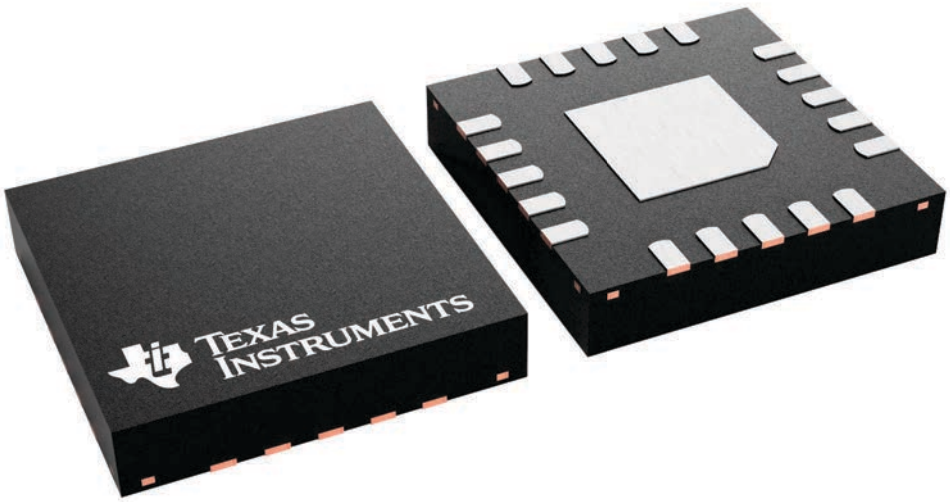
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



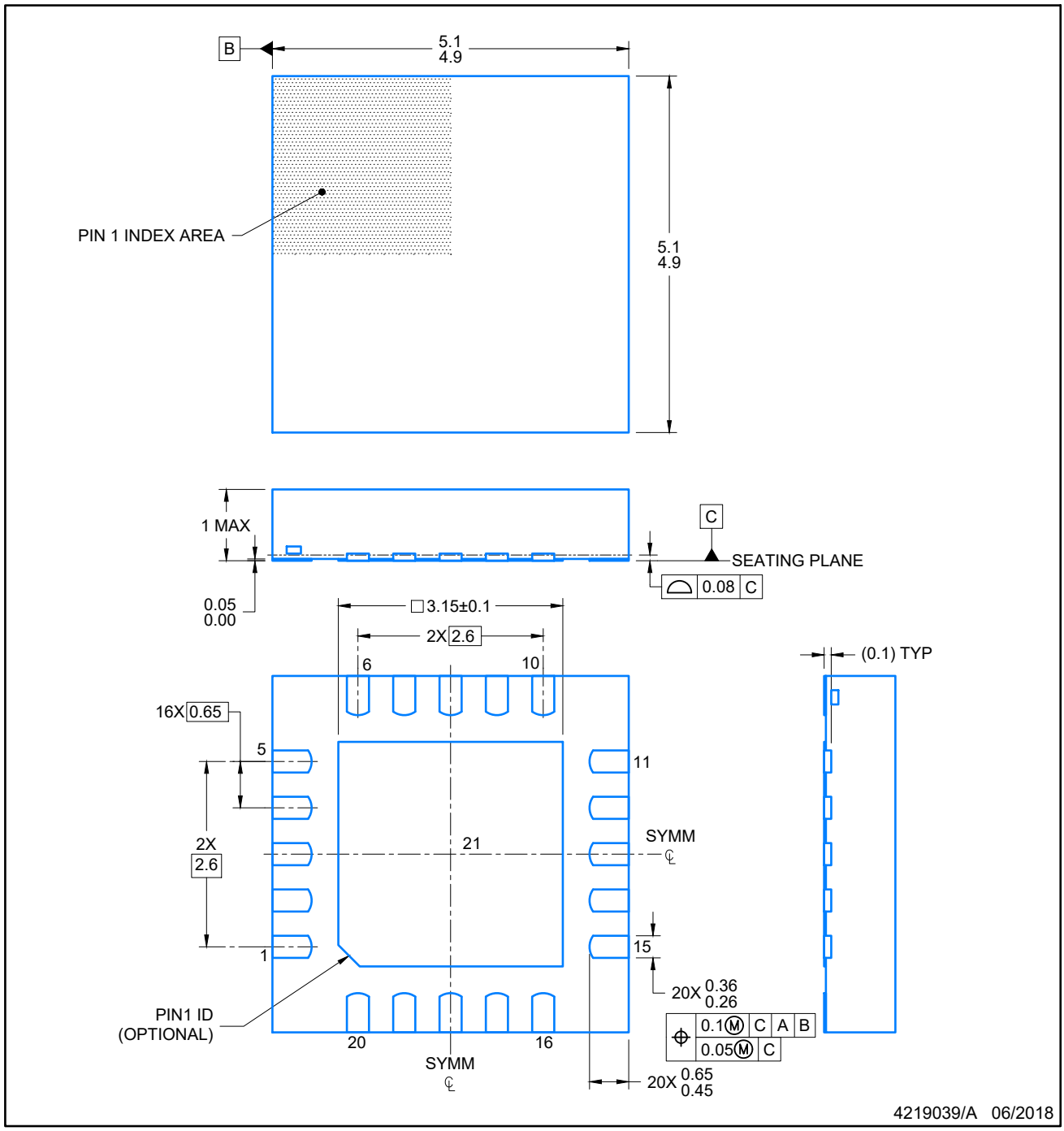
4227157/A

PACKAGE OUTLINE

RGW0020A

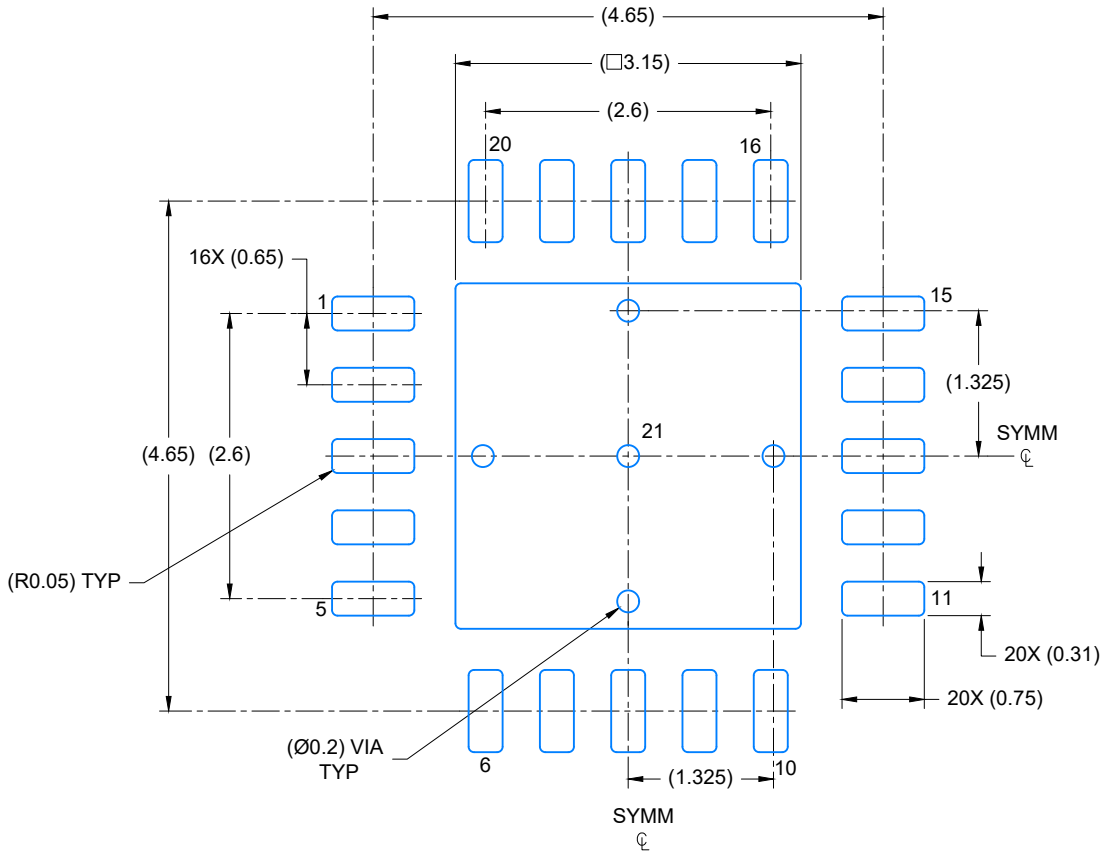
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



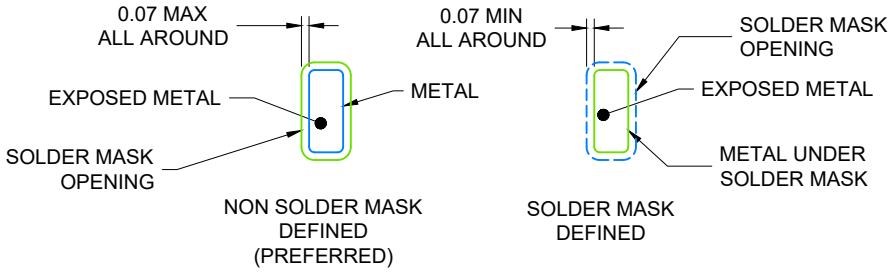
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

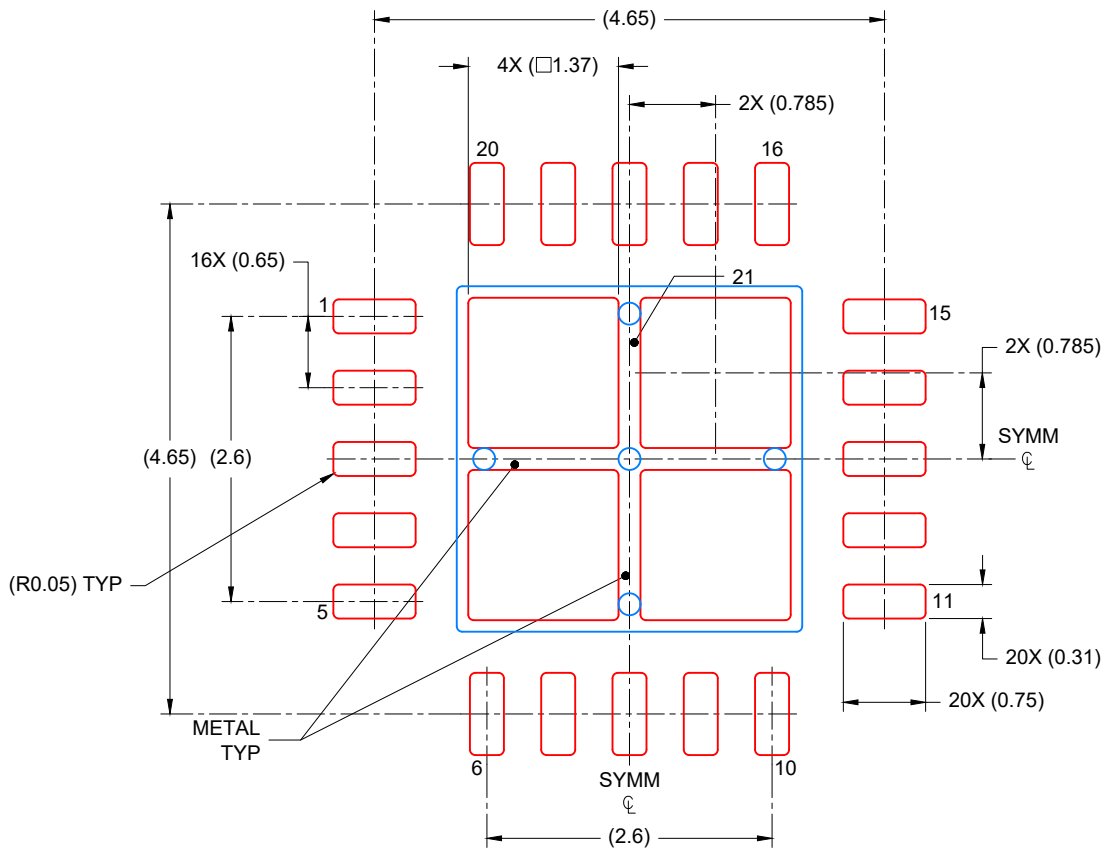


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

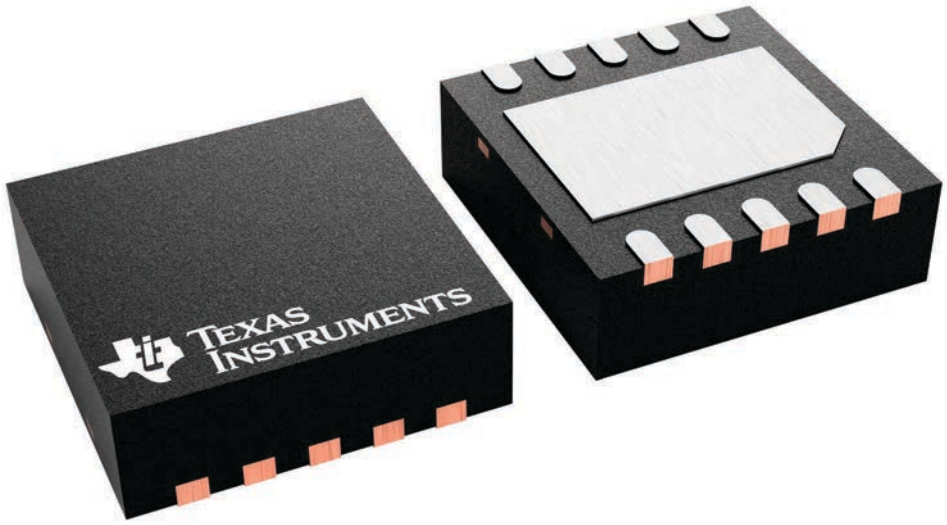
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



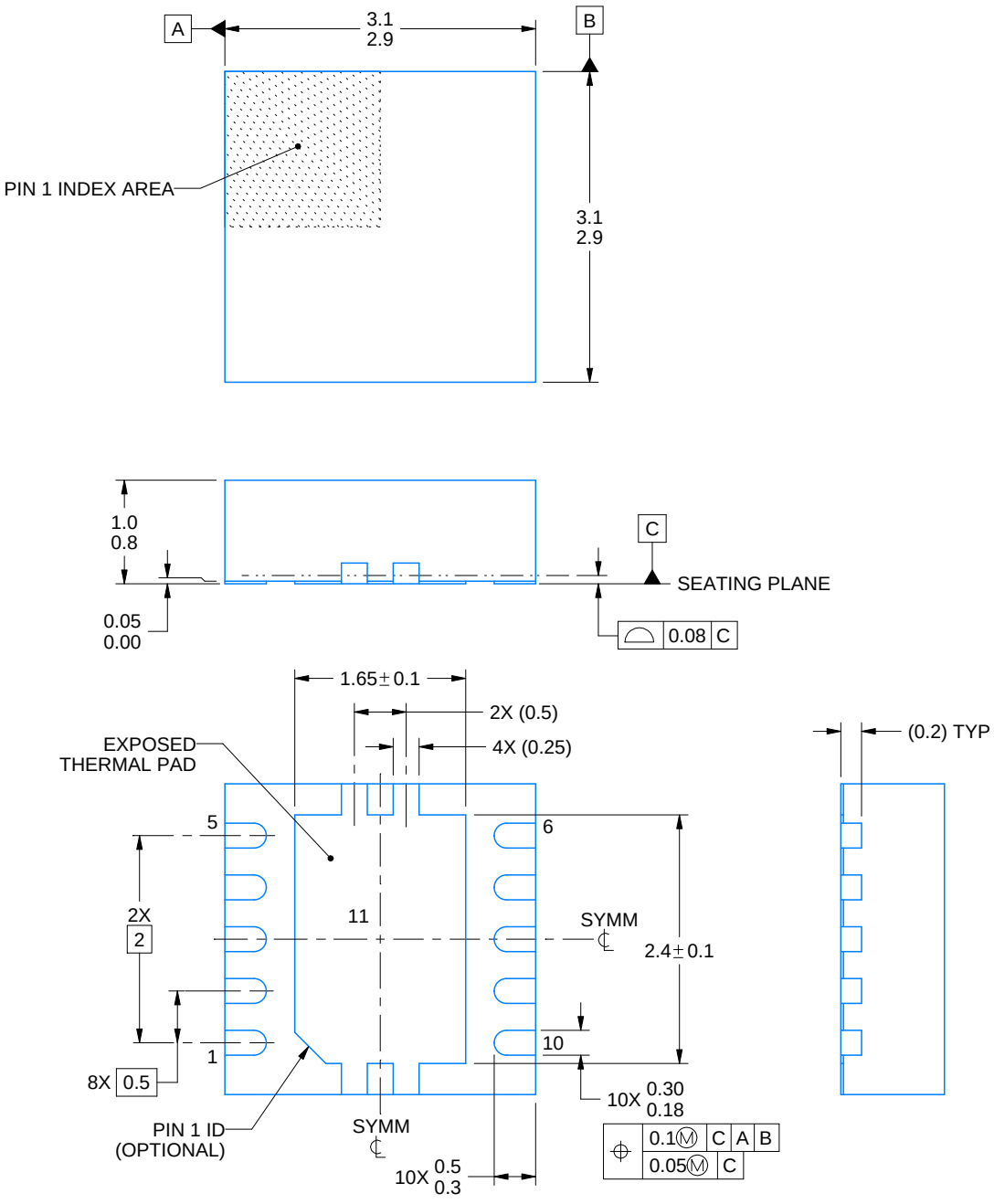
4226193/A

DRC0010J

PACKAGE OUTLINE

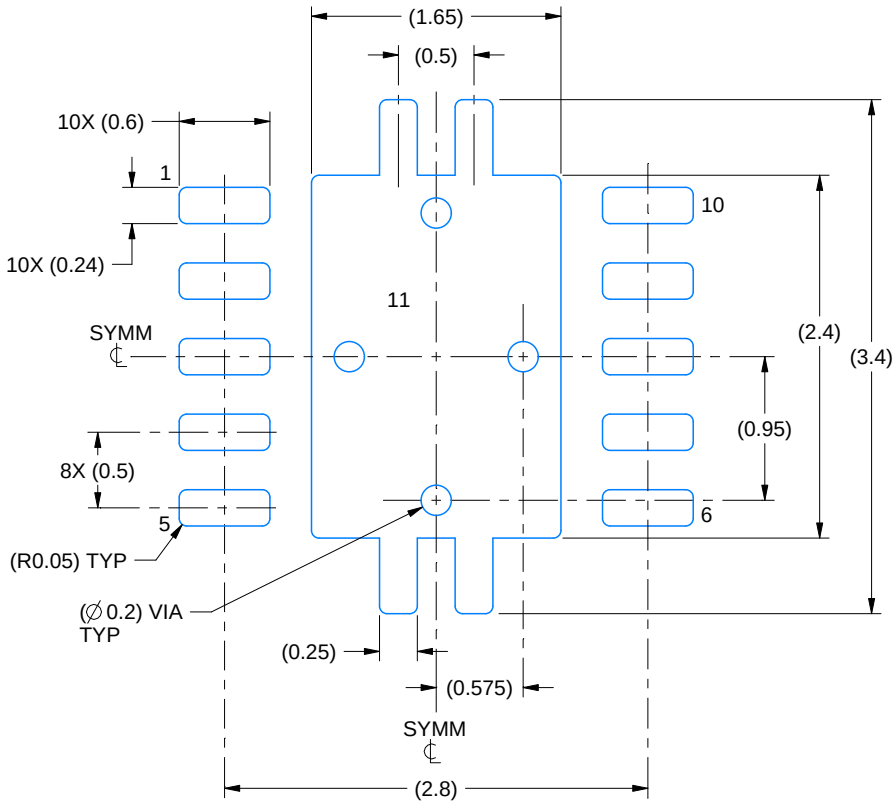
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

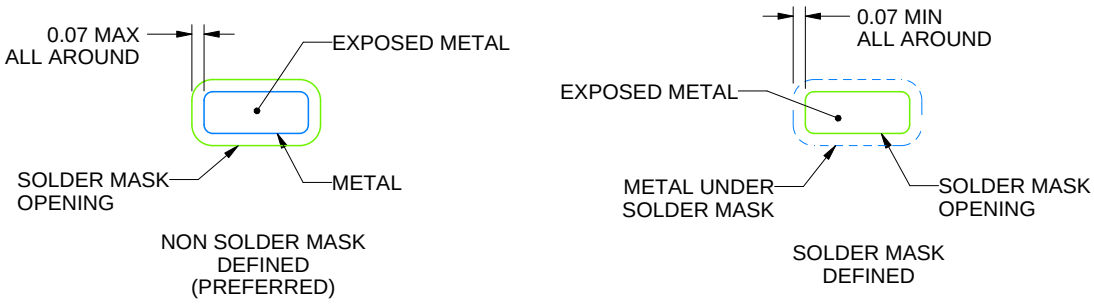


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

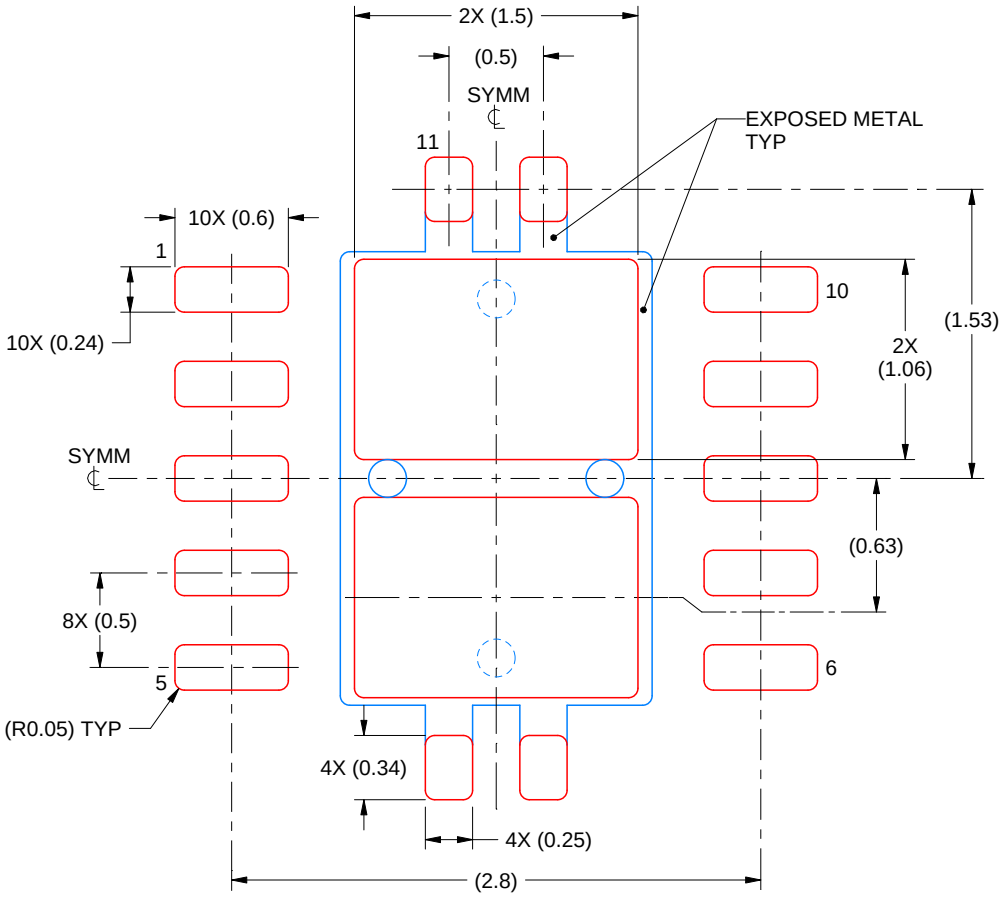
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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