









TPS25948

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TPS25948xx 具有双向电力输送的 3.5V 至 23V、12.2mΩ、8A 电子保险丝

1 特性

- 宽工作输入电压范围: 3.5V 至 23V
 - 绝对最大值为 28V
 - 可以从 IN 或 OUT 供电
- 集成式背对背 FET 具有低导通电阻: R_{ON} = 12.2mΩ(典型值)
- 具有真反向电流阻断功能的理想二极管运行状态 (RCB)
 - 外部引脚控制 (RCBCTRL), 可禁用 RCB 并允 许在稳态下进行双向电力输送,以支持 USB OTG 或 DRP 操作
- 快速过压保护
 - 可调节过压锁定 (OVLO), 响应时间为 1 μs (典 型值)
- 过流保护,具有负载电流监控器输出 (ILM)
 - 有效电流限制响应
 - 可调节阈值 (I_{LIM}) 1A 至 9A
 - I_{LIM} > 3A 时精度为 ±10% (最大值)
 - 可调瞬态消隐计时器 (ITIMER), 支持 > I_{LIM} 的 峰值电流
 - 输出负载电流监控精度:±6%(典型值)(I_{OUT} ≥ 3A)
- 通过快速跳变响应实现短路保护
 - 响应时间 < 1 μs (典型值)
 - 可调节和固定阈值
- 具有可调节欠压锁定阈值 (UVLO) 的高电平有效使 能输入
- 可调节的输出压摆率控制 (dVdt)
- 讨热保护
- 数字输出:电源正常 (SPLYGD/SPLYGD) 和故障指 示 (FLT)
- UL 2367 认证(己计划)
- IEC 62368-1 CB 认证(己计划)
- IEC 61000-4-5: 输入电压为 28V
- 小尺寸: PowerWCSP 2.4mm × 1.7mm, 0.5mm 间距

2 应用

- 适配器和充电器输入保护
- USB PD 保护:智能手机、平板电脑、PC、笔记本 电脑、显示器、扩展坞
- 服务器主板、附加卡
- 企业级存储: HBA、SAN 和 eSSD
- 电源多路复用和 ORing

3 说明

TPS25948xx 系列电子保险丝是采用小型封装的高度集 成电路保护和电源管理解决方案。此类器件提供采用少 量外部元件的多种保护模式,能够非常有效地抵御过 载、短路、电压浪涌和过多浪涌电流。集成式背对背 FET 可帮助阻止从输出端到输入端的反向电流流动, 从而使该器件非常适合电源多路复用器和 ORing 应用 以及需要负载侧能量保持存储解决方案的系统 (如果输 入电源发生故障)。此类器件采用基于线性 ORing 的 方案,可确保实现几乎为零的直流反向电流,并以最小 的正向压降和功率耗散来仿真理想的二极管行为。该器 件还提供了一个外部引脚控制选项,用于禁用反向电流 阻断并允许稳态双向电力输送。

可以使用单个外部电容器来调节输出压摆率和浪涌电 流。通过在输入超过可调过压阈值时切断输出,可以保 护负载免受输入过压情况的影响。此类器件可通过主动 限制电流来应对输出过载。用户可以调节输出电流限值 阈值以及瞬态过流消隐计时器。电流限值控制引脚还用 作模拟负载电流监控器。

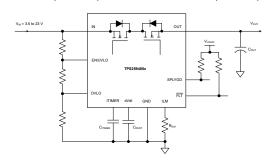
此类器件采用 2.4mm × 1.7mm、12 焊球 Power Wafer Chip Scale Package (PowerWCSP), 旨在改善热性能 并减小系统尺寸。

此类器件的额定工作结温范围为 - 40°C 至 +125°C。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ | | | |
|---------------|-----------------------|---------------------|--|--|--|
| TPS25948xxYWP | YWP (PWCSP , 12) | 2.43mm × 1.71mm | | | |

- (1) 如需了解所有可用型号,请参阅数据表末尾的可订购产品附
- 封装尺寸(长×宽)为标称值,并包括引脚(如适用)。 (2)



简化版原理图



Table of Contents

Product Folder Links: TPS25948

| 1 特性 | 1 |
|--------------------------------------|----------------|
| 2 应用 | 1 |
| 3 说明 | 1 |
| 4 Device Comparison Table | 3 |
| 5 Pin Configuration and Functions | |
| 6 Specifications | |
| 6.1 Absolute Maximum Ratings | <mark>5</mark> |
| 6.2 ESD Ratings | <mark>5</mark> |
| 6.3 Recommended Operating Conditions | 5 |
| 6.4 Thermal Information | 6 |
| 6.5 Electrical Characteristics | 6 |
| 6.6 Timing Requirements | |
| 6.7 Switching Characteristics | |
| 6.8 Typical Characteristics | 11 |
| 7 Detailed Description | 18 |
| 7.1 Overview | |
| 7.2 Functional Block Diagram | |
| 7.3 Feature Description | |
| 7.4 Device Functional Modes | |
| 8 Application and Implementation | 34 |

| 8.1 Application Information | 34 |
|---|----|
| 8.2 Single Device, Self-Controlled | 34 |
| 8.3 Typical Application | 35 |
| 8.4 Active ORing | |
| 8.5 Priority Power MUXing | |
| 8.6 Parallel Operation | |
| 8.7 USB PD Port Protection | |
| 8.8 Power Supply Recommendations | 46 |
| 8.9 Layout | |
| 9 Device and Documentation Support | 50 |
| 9.1 Documentation Support | |
| 9.2 接收文档更新通知 | |
| 9.3 支持资源 | |
| 9.4 Trademarks | |
| 9.5 静电放电警告 | |
| 9.6 术语表 | 50 |
| 10 Revision History | |
| 11 Mechanical, Packaging, and Orderable | |
| Information | 51 |
| | |



4 Device Comparison Table

| Part Number | Steady-state fast-trip threshold | SPLYGD polarity | FLT or RCBCTRL | Response to Fault |
|---------------|------------------------------------|-----------------|----------------|-------------------|
| TPS259480AYWP | | | FLT | Auto-Retry |
| TPS259480LYWP | Adjustable (2 x L) | Active High | FLI | Latch-Off |
| TPS259482AYWP | Adjustable (2 × I _{LIM}) | | | Auto-Retry |
| TPS259482LYWP | | | DODOTO | Latch-Off |
| TPS259481AYWP | Fixed | Active Low | RCBCTRL | Auto-Retry |
| TPS259481LYWP | - Fixed | Active Low | | Latch-Off |

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5 Pin Configuration and Functions

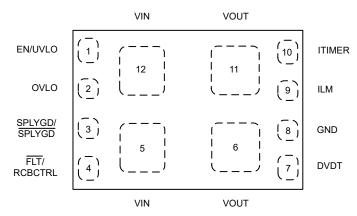


图 5-1. YWP Package, 12-Ball PWCSP (Top View)

表 5-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---------|--------|-------------------|---|
| NAME | NO. | ITPE | DESCRIPTION |
| EN/UVLO | 1 | Analog input | Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the undervoltage lockout threshold. <i>Do not leave floating</i> . Refer to †7.3.1 for details. |
| OVLO | 2 | Analog input | A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an Aactive low enable for the device. <i>Do not leave floating.</i> Refer to † 7.3.2 for details. |
| SPLYGD | 3 | Digital output | TPS259480x/2x: Active high Supply Good indication. This is an open drain signal which is asserted high when the input supply is valid and channel has completed inrush sequence. This can be used to enable/disable the auxiliary supply eFuse to facilitate smooth switchover in a priority power MUXing configuration. Refer to † 7.3.8 for more details. |
| SPLYGD | Digita | | TPS259481x: Active low Supply Good indication. This is an open drain signal which is asserted Low when the input supply is valid and channel has completed inrush sequence. This can be used to enable/disable the auxiliary supply eFuse to facilitate smooth switchover in a priority power MUXing configuration. Refer to † 7.3.8 for more details. |
| FLT | output | | TPS259480x: Active low fault event indicator. This is an open drain signal which will be pulled low when a fault is detected. Refer to † 7.3.7 for more details. |
| RCBCTRL | 4 | Digital input | TPS259481x/2x: Active high reverse current blocking enable input. Leave the pin floating or pull it high to enable reverse current blocking at all times. Pull the pin low to disable reverse current blocking in steady-state to enable bi-directional current flow. |
| IN | 5, 12 | Power | Power input. |
| OUT | 6, 11 | Power | Power output. |
| DVDT | 7 | Analog output | A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to 节 7.3.3.1 for details. |
| GND | 8 | Ground | This is the ground reference for all internal circuits and must be connected to system GND. |
| ILM | 9 | Analog output | This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. <i>Do not leave floating</i> . Refer to 节 7.3.3.2 for more details. |
| ITIMER | 10 | Analog output | A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to † 7.3.3.2 for more details. |

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | Parameter | Pin | MIN | MAX | UNIT |
|--------------------------|--|------------------------|--------------------|------------------------------|------|
| V _{IN,MAX} | Maximum input voltage range, $-40^\circ \text{C} \leqslant T_J \leqslant 125^\circ \text{C}$ | IN | - 0.3 | 28 | V |
| V _{OUT,MAX} | Maximum output voltage range, $$ – $40^{\circ}\!\mathrm{C}\leqslant T_{J} \leqslant 125^{\circ}\!\mathrm{C}$ | OUT | - 0.3 min (2 | 28, V _{IN} + 21) | |
| V _{OUT,MAX} | Maximum output voltage range, -10 $^{\circ}\!$ | OUT | - 0.3 min (2 | 28, V _{IN} + 22) | |
| V _{OUT,MAX,PLS} | Minimum output voltage pulse (< 1 μs) | OUT | - 0.8 | | |
| V _{EN/UVLO,MAX} | Maximum enable pin voltage range | EN/UVLO | - 0.3 | 6.5 | V |
| V _{OVLO,MAX} | Maximum OVLO pin voltage range | OVLO | - 0.3 | 6.5 | V |
| $V_{dVdt,MAX}$ | Maximum dVdT pin voltage range | dVdt | Internally limited | | V |
| V _{ITIMER,MAX} | Maximum ITIMER pin voltage range | ITIMER | Internally limited | | V |
| V _{RCBCTRL,MAX} | Maximum RCBCTRL pin voltage range | RCBCTRL | - 0.3 | 6.5 | V |
| V _{SPLYGD,MAX} | Maximum SPLYGD/SPLYGD pin voltage range | SPLYGD/SPLYGD | - 0.3 | 6.5 | V |
| V _{FLTB,MAX} | Maximum FLT pin voltage range | FLT | - 0.3 | 6.5 | V |
| V _{ILM,MAX} | Maximum ILM pin voltage range | ILM | Internally limited | | V |
| I _{MAX} | Maximum continuous switch current | IN to OUT or OUT to IN | Internally limited | | Α |
| T _{J,MAX} | Maximum operating junction temperature | | Internally limited | | °C |
| T _{LEAD,MAX} | Maximum lead temperature | | | 300 | °C |
| T _{STG,MAX} | Maximum storage temperature | | - 65 | 150 | °C |

⁽¹⁾ Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V.===\ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| V _(ESD) | Liectiostatic discharge | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±500 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | Parameter | Pin | MIN | MAX | UNIT |
|----------------------|-------------------------------|---------|--------------------------------------|-----------------------------------|------|
| V _{IN} | Input voltage range | IN | 3.5 | 23 | V |
| V _{OUT} | Output voltage range | OUT | | min (23, V _{IN} + 20) | V |
| V _{EN/UVLO} | Enable pin voltage range | EN/UVLO | | 5 ⁽¹⁾ | V |
| V _{OVLO} | OVLO pin voltage range | OVLO | 0.5 | 1.5 | V |
| V_{dVdt} | dVdT capacitor voltage rating | dVdt | V _{IN} + 5 V ⁽²⁾ | | V |
| V _{RCBCTRL} | RCBCTRL pin voltage range | RCBCTRL | | 5 | V |
| V _{FLTB} | FLTB pin voltage range | FLTB | | 5 | V |

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6.3 Recommended Operating Conditions (续)

over operating free-air temperature range (unless otherwise noted)

| | <u> </u> | · · · · · · · · · · · · · · · · · · · | | | |
|---------------------|--|---------------------------------------|------|------|------|
| | Parameter | Pin | MIN | MAX | UNIT |
| V _{SPLYGD} | SPLYGD/SPLYGD pin voltage range | SPLYGD/SPLYGD | | 5 | V |
| V _{ITIMER} | ITIMER pin capacitor voltage rating | ITIMER | 4 | | V |
| R _{ILM} | ILM pin resistance | ILM | 536 | 4834 | Ω |
| I _{LOAD} | Continuous switch current, $T_J \leqslant 125^{\circ}\!$ | IN to OUT or OUT to IN | | 8 | Α |
| T _J | Junction temperature | | - 40 | 125 | °C |

⁽¹⁾ For supply voltages below 5 V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5 V, it is recommended to use a resistor divider to step down the voltage.

6.4 Thermal Information

| | THERMAL METRIC (1) | TPS25948xx YWP (PWCSP) 12 PINS | UNIT |
|-------------------|--|--------------------------------------|------|
| R ₀ JA | Junction-to-ambient thermal resistance | 33.4 ⁽²⁾ | °C/W |
| $\Psi_{\sf JT}$ | Junction-to-top characterization parameter | 0.3 ⁽²⁾ | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 11.2 ⁽²⁾ | °C/W |

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) $-40^{\circ}\text{C} \leqslant T_{J} \leqslant 125^{\circ}\text{C}$, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, V_{ILM} = 536 Ω , dVdT = Open, ITIMER = Open, SPLYGD/SPLYGD = Open, FLT = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x. All voltages referenced to GND.

| Test Parameter | Description | MIN | TYP | MAX | UNITS |
|----------------------------------|--|-----|-----|------|-------|
| INPUT SUPPL | Y (IN) | | | | |
| V _{UVP(R),IN} | IN supply undervoltage protection rising threshold | 2.7 | 3.0 | 3.3 | V |
| V _{UVP(F),IN} | IN supply undervoltage protection falling threshold | 2.2 | 2.4 | 2.65 | V |
| I _{Q(ON,IN)} | IN supply ON state quiescent current when powered from IN, $V_{EN} > V_{UVLO(R)}$ | | 439 | 640 | μΑ |
| I _{Q(OFF,UVLO,IN)} | IN supply OFF state current when powered from IN, $V_{SD(F)} < V_{EN} < V_{UVLO(R)}$ | | 73 | 193 | μΑ |
| I _{OUTLKG(ON)} | OUT supply leakage current when powered from IN | | 432 | 640 | μΑ |
| I _{OUTLKG(OFF)} | OUT supply leakage current when powered from IN, UVLO condition (V _{SD(F)} < V _{EN} < V _{UVLO(R)}) | | 7 | 29 | μΑ |
| I _{SD(IN)} | IN supply shutdown current when powered from IN, $V_{EN} < V_{SD(F)}$ | | 7 | 12 | μΑ |
| $V_{UVP(R),OUT}$ | OUT supply undervoltage protection rising threshold | 2.7 | 3.0 | 3.3 | V |
| V _{UVP(F),OUT} | OUT supply undervoltage protection falling threshold | 2.2 | 2.4 | 2.65 | V |
| OUTPUT SUP | PLY (OUT) | | | | |
| I _{Q(ON,OUT)} | OUT supply ON state quiescent current when powered from OUT, V _{EN} > V _{UVLO(R)} | | 422 | 640 | μΑ |
| I _{Q(OFF,UVLO,OU} T) | OUT supply OFF state current when powered from OUT, V _{SD(F)} < V _{EN} < V _{UVLO(R)} | | 71 | 110 | μΑ |

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⁽²⁾ In a PowerMUX scenario with unequal supplies, the dVdt capacitor rating for each device should be chosen based on the highest of the 2 rails.

⁽²⁾ Custom PCB layout 2s2p

6.5 Electrical Characteristics (续)

(Test conditions unless otherwise noted) $-40^{\circ}\text{C} \leqslant \text{T}_{\text{J}} \leqslant 125^{\circ}\text{C}, \text{V}_{\text{IN}} = 12 \text{ V}, \text{OUT} = \text{Open}, \text{V}_{\text{EN/UVLO}} = 2 \text{ V}, \text{V}_{\text{OVLO}} = 0 \text{ V}, \text{R}_{\text{ILM}} = 536 \ \Omega$, dVdT = Open, ITIMER = Open, SPLYGD/SPLYGD = Open, FLT = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x. All voltages referenced to GND.

| Test Parameter | Description | MIN | TYP | MAX | UNITS |
|-----------------------|--|--------|--------|--------|---------------------|
| SD(OUT) | OUT supply shutdown current when powered from OUT, V _{EN} < V _{SD(F)} | | 7 | 29 | μΑ |
| ON RESISTAN | NCE (IN - OUT) | | | | |
| | V _{IN} = 12 V, I _{OUT} = 3 A, T _J = 25°C | | 12.2 | 15 | mΩ |
| R _{ON} | $3.5 \leqslant V_{\text{IN}} \leqslant 23 \text{ V}, I_{\text{OUT}} = 3 \text{ A}, -40 ^{\circ}\!$ | | | 20 | mΩ |
| ENABLE/UND | PERVOLTAGE LOCKOUT (EN/UVLO) | | | | |
| V _{UVLO(R)} | EN/UVLO pin rising threshold to turn FET ON | 1.17 | 1.2 | 1.23 | V |
| / _{UVLO(F)} | UVLO pin falling threshold to turn FET OFF | 1.07 | 1.1 | 1.12 | V |
| / _{SD(F)} | EN/UVLO falling threshold for lowest shutdown current | 0.54 | 0.75 | | V |
| ENLKG | EN/UVLO pin leakage current | - 0.1 | | 0.1 | μA |
| OVERVOLTA | GE LOCKOUT (OVLO) | | | | |
| V _{OV(R)} | OVLO pin rising threshold | 1.18 | 1.2 | 1.23 | V |
| / _{OV(F)} | OVLO pin falling threshold | 1.07 | 1.1 | 1.12 | V |
| OVLKG | OVLO pin leakage current, 0.5 V < V _{OVLO} < 1.5 V | - 0.1 | | 0.1 | μA |
| OUTPUT LOA | D CURRENT MONITOR (IMON) | | | | |
| G _{IMON} | Analog load current monitor gain (IMON : IOUT), I _{OUT} = 1 A, I _{OUT} < I _{LIM} | 114 | 133 | 154 | μΑ/Α |
| SIMON | Analog load current monitor gain (IMON : IOUT), I _{OUT} = 3 A to 8 A, I _{OUT} < I _{LIM} | 116 | 133 | 149 | μΑ/Α |
| OVERCURRE | NT PROTECTION (OUT) | | | | |
| | Overcurrent threshold, R_{ILM} = 2.43 k Ω | 1.75 | 1.99 | 2.25 | Α |
| LIM | Overcurrent threshold, R_{ILM} = 1.62 k Ω | 2.7 | 2.98 | 3.3 | Α |
| | Overcurrent threshold, R_{ILM} = 604 Ω | 7.2 | 8 | 8.7 | Α |
| | Circuit-breaker threshold, ILM pin open (Single point failure) | | | 0.1 | Α |
| FLT | Circuit-breaker threshold, ILM pin shorted to GND (Single point failure) | | 1.4 | 2.5 | А |
| SCGain | Scalable Fast-trip current threshold (I _{SC}) : I _{LIM} Ratio (Steady-state/Start-up for TPS259480x/2x variants and Start-up for TPS259481x variants) | 170% | 184% | 240% | |
| FFT | Fixed Fast-trip current threshold, TPS259480x/2x variants only | 16.9 | 25.1 | 31.0 | Α |
| | Fixed Fast-trip current threshold, TPS259481x variants only | 15 | 22.8 | 29 | Α |
| / _{FB} | V _{OUT} threshold to exit current limit foldback | 1.5 | 1.9 | 2.3 | V |
| | NT FAULT TIMER (ITIMER) | | | | |
| / _{INT} | ITIMER pin internal pull-up voltage | 2.3 | 2.6 | 2.7 | V |
| RITIMER | ITIMER pin internal pull-up resistance | | 15.7 | | $\mathbf{k} \Omega$ |
| ITIMER | ITIMER pin discharge current, I _{OUT} > I _{LIM} | 1.5 | 1.9 | 2.45 | μΑ |
| ∆ V _{ITIMER} | ITIMER discharge differential voltage threshold | 1.28 | 1.51 | 1.75 | V |
| REVERSE CU | RRENT BLOCKING (IN - OUT) | | | | |
| / _{FWD} | V _{IN} - V _{OUT} forward regulation voltage, I _{OUT} = 10 mA | 0.1 | 10.6 | 24.5 | mV |
| √ _{REVTH} | V _{IN} - V _{OUT} threshold for fast BFET turn off (enter reverse current blocking) | - 44.8 | - 29.5 | - 14.8 | mV |

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English Data Sheet: SLVSGT9



6.5 Electrical Characteristics (续)

(Test conditions unless otherwise noted) $-40^{\circ}\text{C} \leqslant \text{T}_{\text{J}} \leqslant 125^{\circ}\text{C}$, V_{IN} = 12 V, OUT = Open, $\text{V}_{\text{EN/UVLO}}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 536 Ω , dVdT = Open, ITIMER = Open, SPLYGD/SPLYGD = Open, FLT = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x. All voltages referenced to GND.

| Test Parameter | Description | | TYP | MAX | UNITS |
|-------------------------|--|--------|-------|------|-------|
| V _{FWDTH} | V _{IN} - V _{OUT} threshold for fast BFET turn on (exit reverse current blocking) | 70 | 105.9 | 140 | mV |
| I _{REVLKG} | Reverse leakage current during reverse current blocking condition | - 2 | - 1.1 | | μА |
| SUPPLY GOO | D INDICATION (SPLYGD/SPLYGD) | | | • | |
| V _{SPLYGD} | SPLYGD pin low voltage V _{IN} > 3.3V, Strong pull-up | | | 600 | mV |
| V _{SPLYGD} | SPLYGD pin low voltage V_{IN} < 3.3V, EN < $V_{SD(F)}$, weak pullup | | 650 | 930 | mV |
| V _{SPLYGD} | SPLYGD pin low voltage V_{IN} < 3.3V, EN < $V_{SD(F)}$, strong pullup | | 785 | 990 | mV |
| I _{SPLYGDLKG} | SPLYGD High leakage current - 3 | | 3 | μA | |
| I _{SPLYGDBLKG} | SPLYGD High leakage current | - 3 | | 3 | μA |
| FAULT INDIC | ATION (FLT) or REVERSE BLOCKING CONTROL (RCBCTRL) | | | ' | |
| I _{FLTBLKG} | FLT leakage current | - 1 | | 1 | μA |
| R _{FLTB} | FLT pin internal pull-down resistance, TPS259480x variants only | s 11.8 | | Ω | |
| I _{RCBCTRL} | RCBCTRL pin internal pull-up current, TPS259481x/2x variants only | 5 | | μΑ | |
| V _{IH,RCBCTRL} | RCBCTRL pin logic high detection threshold, TPS259481x/2x variants only | 1.09 | 1.15 | 1.2 | V |
| V _{IL,RCBCTRL} | RCBCTRL pin logic low detection threshold, TPS259481x/2x variants only | 1.0 | 1.0 | 1.11 | V |
| OVERTEMPE | RATURE PROTECTION (OTP) | | | | |
| TSD | Thermal shutdown rising threshold, T _J rising | | 154 | | °C |
| TSD _{HYS} | Thermal shutdown hysteresis, T _J falling | 10 | | | °C |
| SLEW RATE | CONTROL (DVDT) | | | · | |
| l _{dvdt} | dVdt pin charging current | 2.6 | 5.3 | 9 | μA |
| | | | | | |

6.6 Timing Requirements

| | PARAMETER | TEST CONDITIONS | MIN TYP MAX | UNIT |
|----------------------|---|--|-------------|------|
| t _{OVLO} | Overvoltage lock-out response time | V _{OVLO} > V _{OV(R)} to V _{OUT} ↓ | 1 | μs |
| t _{LIM} | Current limit response time | $I_{\rm OUT}$ > 1.2 × $I_{\rm LIM}$ and ITIMER expired to $I_{\rm OUT}$ settling to within 5% of $I_{\rm LIM}$ | 250 | μs |
| t _{sc} | Scalable fast-trip response time (TPS259480x/2x only) | I _{OUT} > 3 × I _{LIM} to I _{OUT} ↓ | 900 | ns |
| t _{FT} | Fixed fast-trip response time | I _{OUT} > I _{FFT} to I _{OUT} ↓ | 750 | ns |
| t _{RST} | Auto-Retry interval after fault (TPS25948xA only) | | 103 | ms |
| t _{SWOV} | OVLO fast recovery response time | V _{OVLO} < V _{OV(F)} to V _{OUT} ↑ | 85.3 | μs |
| t _{SWRCB} | Reverse Current Blocking recovery time | $(V_{IN} - V_{OUT}) > V_{FWDTH}$ to $V_{OUT} \uparrow$ | 46.5 | μs |
| t _{RCB} | Reverse Current Blocking comparator response time | (V _{OUT} - V _{IN}) > 1.3 × V _{REVTH} to BFET OFF | 1.1 | μs |
| t _{SPLYGDA} | Supply Good assertion de-glitch | | 14.7 | μs |

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6.6 Timing Requirements (续)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|------------------------------------|-----------------|-----|------|-----|------|
| t _{SPLYGDD} | Supply Good de-assertion de-glitch | | | 14.3 | | μs |

9

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6.7 Switching Characteristics

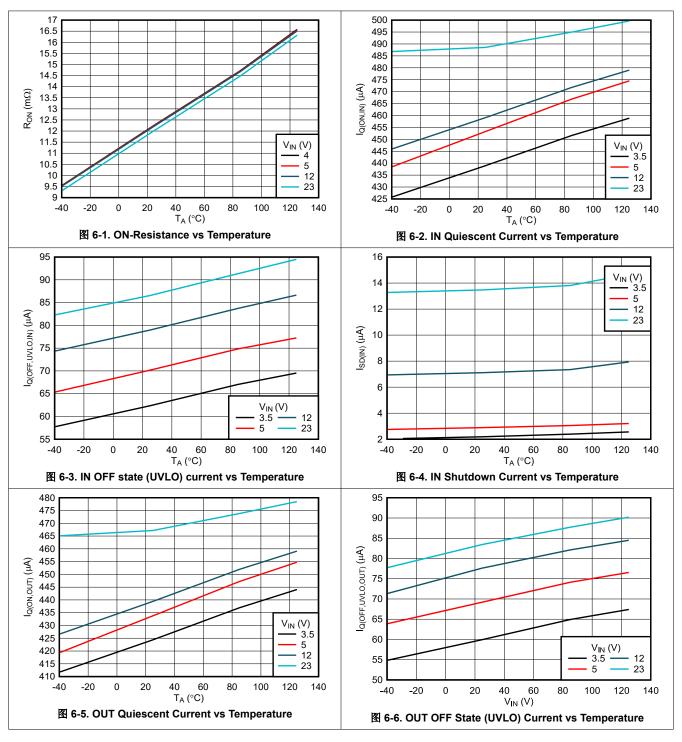
The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at $T_J = 25^{\circ}C$ unless specifically noted otherwise. $R_{OUT} = 100 \Omega$, $C_{OUT} = 1 \mu F$

| | PARAMETER | VIN | C _{dVdt} = Open | C _{dVdt} = 3.3 nF | C _{dVdt} = 6.8 nF | UNITS |
|--------------------|-------------------------|-----|--|----------------------------|----------------------------|-------|
| | | 3.5 | 0.15 | 0.78 | 1.31 | ms |
| $t_{D,ON}$ | Turn on delay | 12 | 0.17 | 1.04 | 2.04 | ms |
| | | 23 | 0.18 | 1.60 | 3.44 | ms |
| | | 3.5 | 14.40 | 1.25 | 0.58 | V/ms |
| SR _{ON} | Output rising slew rate | 12 | 25.30 | 1.36 | 0.60 | V/ms |
| | 1.515 | 23 | 38.30 | 1.44 | 0.65 | V/ms |
| | | 3.5 | 0.20 | 2.12 | 4.59 | ms |
| t _R | Rise time | 12 | 0.36 | 7.04 | 17.08 | ms |
| | | 23 | 0.47 | 12.83 | 27.70 | ms |
| | | 3.5 | 0.41 | 2.88 | 5.89 | ms |
| t _{ON} | Turn on time | 12 | 0.55 | 8.09 | 19.14 | ms |
| | | 23 | 0.65 | 14.66 | 31.20 | ms |
| | | 3.5 | 17.30 | 17.30 | 17.30 | μs |
| t _{D,OFF} | Turn off delay | 12 | 15.80 | 15.80 | 15.80 | μs |
| | | 23 | 13.50 | 13.50 | 13.50 | μs |
| t _F | Fall time | 3.5 | | | | |
| | | 12 | Depends on R _{OUT} and C _{OUT} | | μs | |
| | | 23 | | | | |

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6.8 Typical Characteristics

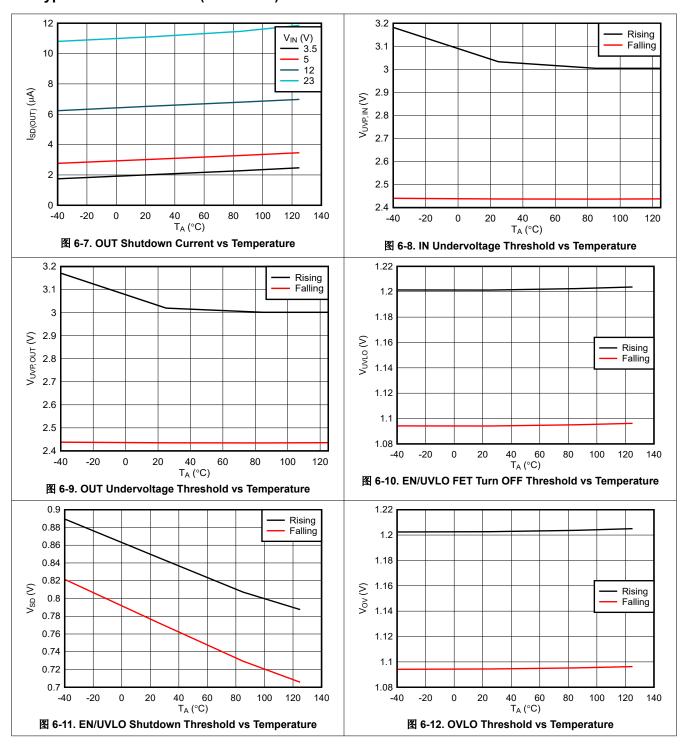


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11

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12

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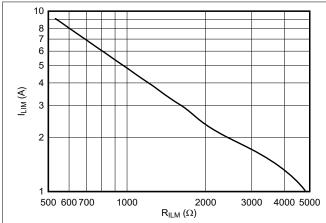


图 6-13. Overcurrent Threshold vs ILM Resistor

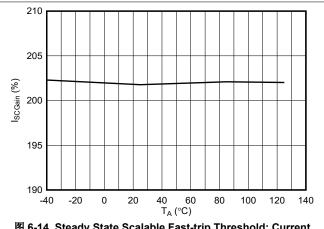


图 6-14. Steady State Scalable Fast-trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature (TPS259480x/2x)

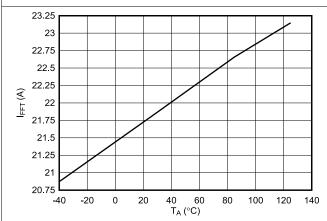


图 6-15. Steady State Fixed Fast-Trip Current Threshold vs Temperature (TPS259481x)

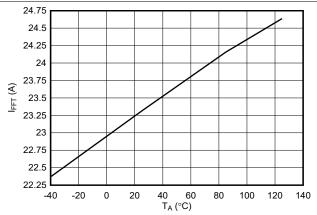
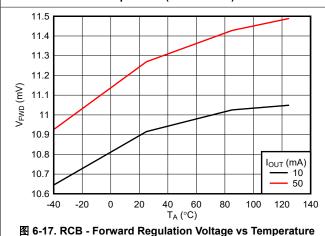


图 6-16. Steady State Fixed Fast-Trip Current Threshold vs Temperature (TPS259480x/2x)



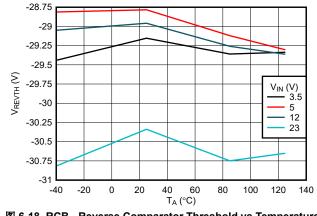


图 6-18. RCB - Reverse Comparator Threshold vs Temperature

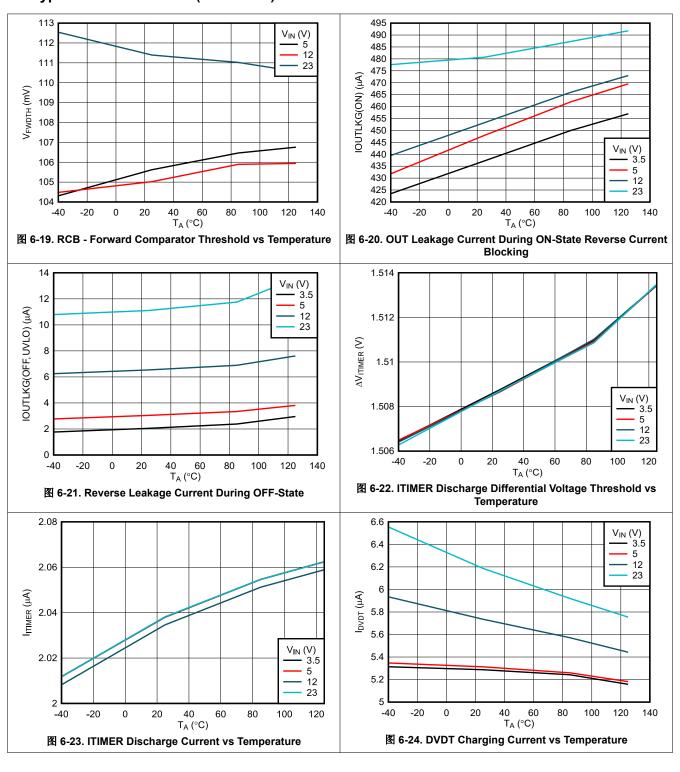
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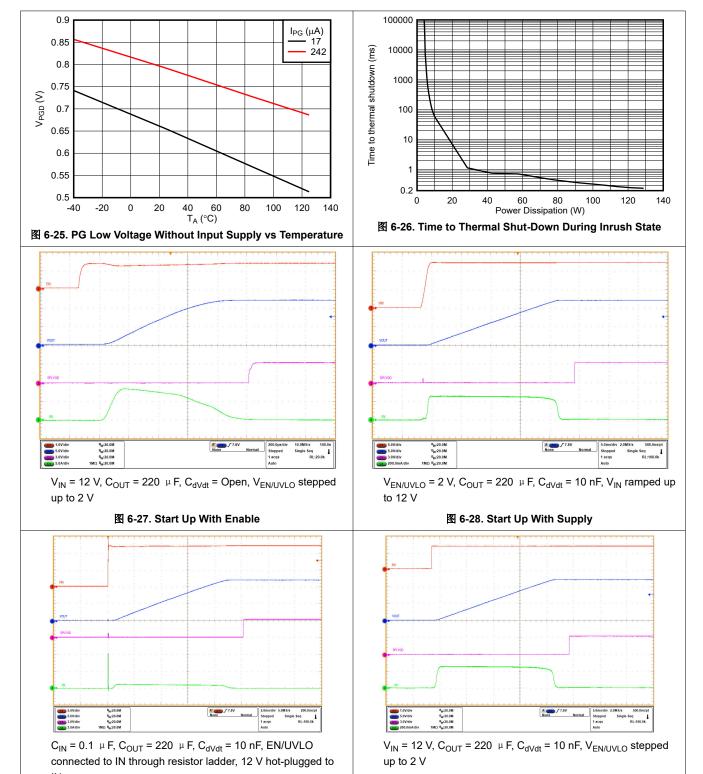
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13

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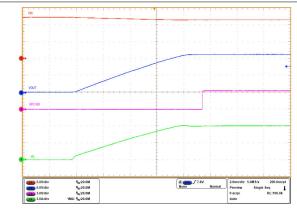
图 6-29. Input Hot-Plug

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15

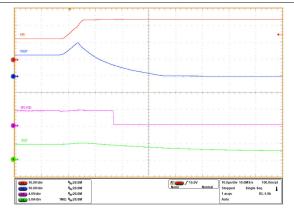
图 6-30. Inrush Current With Capacitive Load





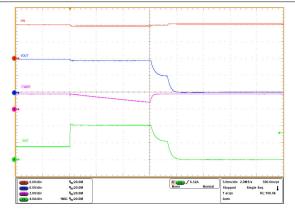
 V_{IN} = 12 V, C_{OUT} = 220 $\,\mu$ F, R_{OUT} = 2 $\,\Omega$, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 2 V

图 6-31. Inrush Current With Resistive and Capacitive Load



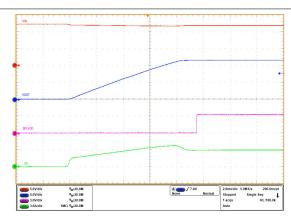
 V_{IN} Overvoltage threshold set to 20 V, V_{IN} ramped up from 12 V to 23 V

图 6-33. Overvoltage Lockout Response



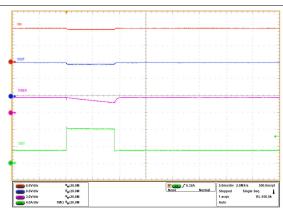
 V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 220 $\,\mu$ F, I_{LIM} set to 4.5 A, I_{OUT} stepped from 3 A \rightarrow 9 A

图 6-35. Active Current Limit Response Followed by TSD



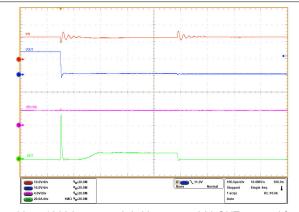
 V_{IN} = 12 V, C_{OUT} = 690 $~\mu$ F, R_{OUT} = 4 $~\Omega$, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 2 V

图 6-32. Inrush Current With Resistive and Capacitive Load



 V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 220 $\,\mu$ F, I_{LIM} set to 4.5 A, I_{OUT} ramped from 3 A \rightarrow 8 A \rightarrow 3 A within 9 ms

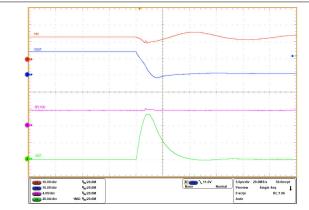
图 6-34. Transient Overcurrent Blanking Timer Response



 V_{IN} = 12 V, I_{LIM} set to 9 A, $V_{EN/UVLO}$ = 2 V, OUT stepped from Open \rightarrow Short-circuit to GND

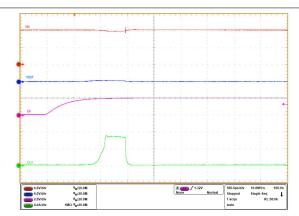
图 6-36. Output Short-Circuit During Steady State

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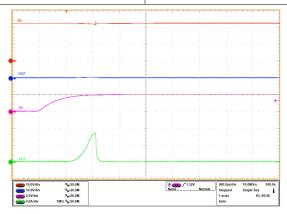
 V_{IN} = 12 V, I_{LIM} set to 9 A, $V_{EN/UVLO}$ = 2 V, OUT stepped from Open \rightarrow Short-circuit to GND

图 6-37. Output Short-Circuit During Steady State (Zoomed In)



 V_{IN} = 12 V, OUT short-circuit to GND, I_{LIM} set to 4.5 A, $V_{\text{EN}/\text{UVLO}}$ stepped from 0 V to 2 V

图 6-38. Power Up Into Short-Circuit



 V_{IN} = 22 V, OUT short-circuit to GND, I_{LIM} set to 9 A, $V_{EN/UVLO}$ stepped from 0 V to 2 V

图 6-39. Power Up Into Short-Circuit



7 Detailed Description

7.1 Overview

The TPS25948xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN and OUT bus voltage. When the supply voltage (V_{IN} or V_{OUT}) exceeds the Undervoltage Protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow between IN and OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off to block current flow between IN and OUT.

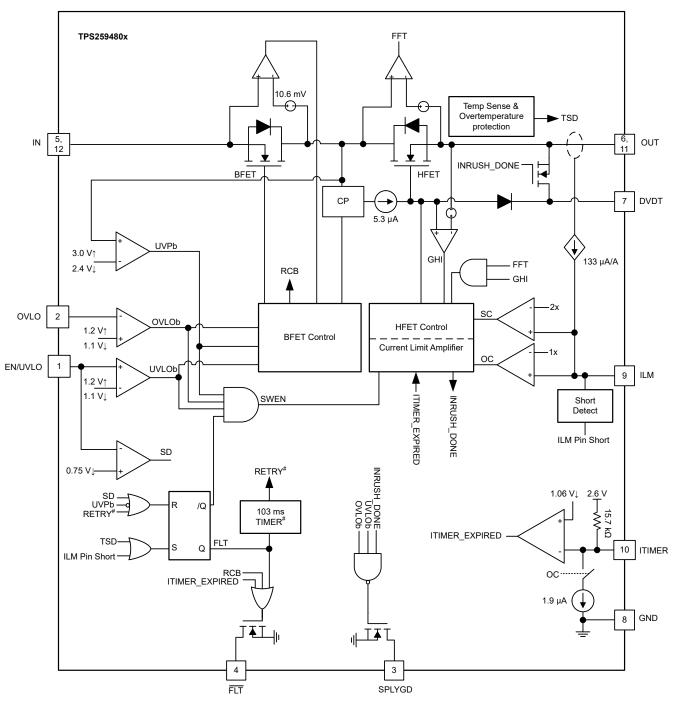
After a successful start-up sequence, the device now actively monitors its load current and bus voltage and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are cut-off once they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (V_{FWD}) in forward conduction mode and turned off completely to block reverse current if output voltage exceeds the input voltage. In some device variants, the reverse current blocking can be disabled using an external pin control (RCBCTRL) to allow bi-directional current flow to support applications such as USB On-the-go or DRP (Dual Role Port).

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

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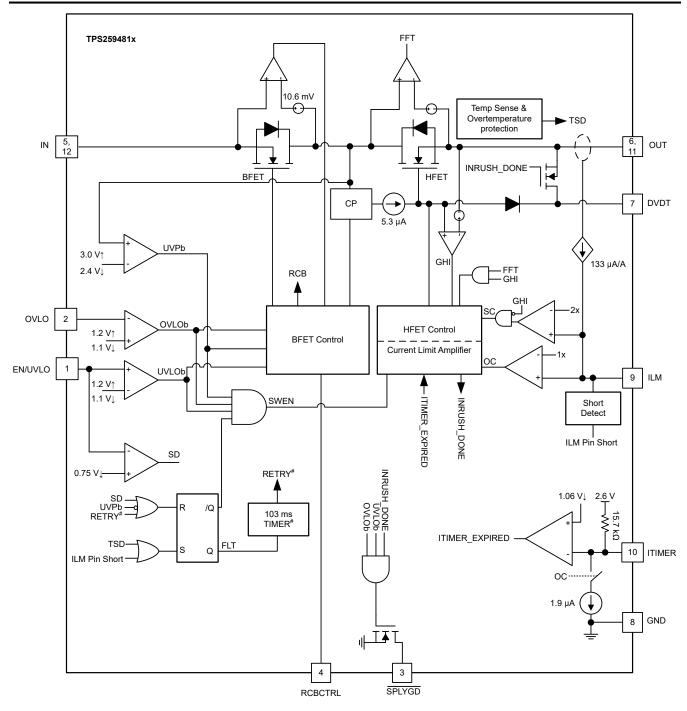
7.2 Functional Block Diagram



Not applicable to Latch-off variant (TPS259480L)

图 7-1. TPS259480x Block Diagram



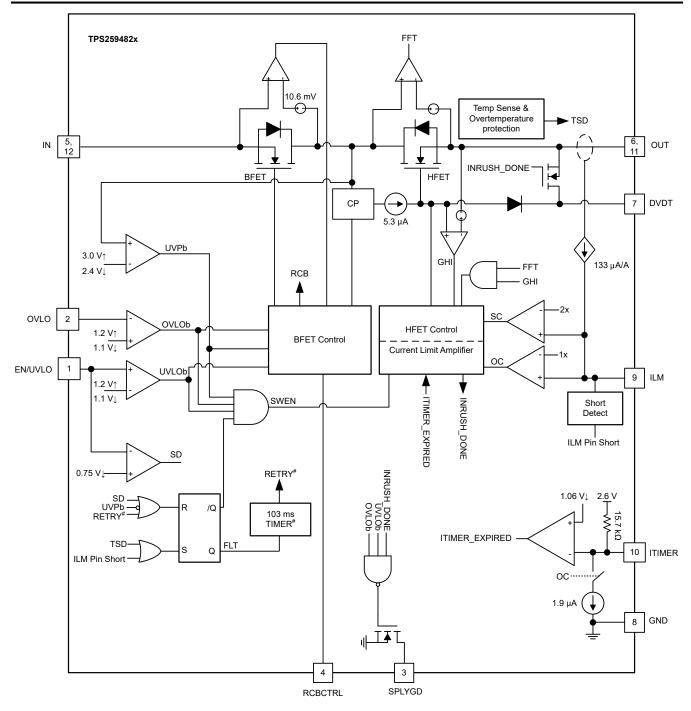


Not applicable to Latch-off variant (TPS259481L)

图 7-2. TPS259481x Block Diagram

20

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Not applicable to Latch-off variant (TPS259482L)

图 7-3. TPS259482x Block Diagram

7.3 Feature Description

The TPS25948xx eFuse is a compact, feature rich power management device that provides detection, protection, and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS25948xx implements undervoltage protection on IN and OUT in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. 图 7-4 and 方程式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

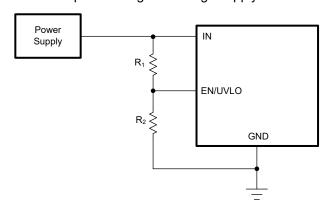


图 7-4. Adjustable Undervoltage Protection

$$VIN(UV) = VUVLO(F) \times \frac{R1 + R2}{R2}$$
 (1)

7.3.2 Overvoltage Lockout (OVLO)

The TPS25948xx allows the user to implement Overvoltage protection on the bus to shield the system against supply overvoltage conditions. The internal fast comparator on the OVLO pin allows the Overvoltage Lockout threshold to be adjusted to a user defined value. Once the voltage at the OVLO pin crosses the OVLO rising threshold V_{OV(R)}, the device turns off both the FETs to cut off the power path. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the FETs are turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. 图 7-5 and 方程式 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

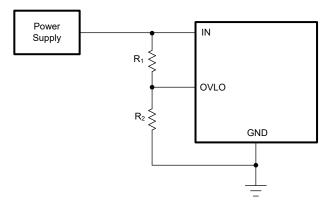


图 7-5. Adjustable Overvoltage Protection

$$VIN(OV) = VOV(F) \times \frac{R1 + R2}{R2}$$
 (2)

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While recovering from a OVLO event, the TPS25948xx bypasses the inrush control (dVdt) and starts up in a current limited manner to provide faster turn ON and minimize power supply droop during supply transient conditions.

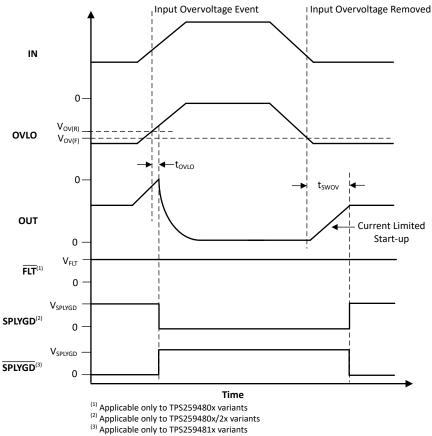


图 7-6. TPS25948xx Overvoltage Lockout and Recovery

7.3.3 Inrush Current, Overcurrent, and Short Circuit Protection

TPS25948xx incorporates four levels of protection against overcurrent:

- 1. Adjustable slew rate (dVdt) for inrush current control
- 2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
- 3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
- 4. Fixed threshold (I_{FFT}) for fast-trip response to quickly protect against hard output short-circuits during steadystate

7.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

方程式 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$IINRUSH (mA) = COUT (\mu F) \times SRON (V/ms)$$
(3)

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the equation:

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CDVDT (pF) =
$$\frac{5000}{\text{SRON} (\text{V/ms})}$$
 (4)

The fastest output slew rate is achieved by leaving the dVdt pin open.

备注

- 1. The slew rate calculation above holds good for $C_{dVdt} > 1$ nF. For lower C_{dVdt} values, the internal gate capacitance may dominate and cause the actual slew rate to deviate from the calculation.
- 2. Slew rate control during start-up is provided only on the HFET which enables inrush current control from IN to OUT.
- 3. For C_{dVdt} > 10 nF, it is recommended to add a 100- Ω resistor in series with the capacitor on the dVdt pin.

7.3.3.2 Active Current Limiting

The TPS25948xx responds to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold ($2 \times I_{LIM}$ or I_{FFT} depending on the variant), the device starts discharging the ITIMER pin capacitor using an internal 1.9- μ A pulldown current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER} , the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This allows short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and once it discharges by ΔV_{ITIMER} , the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. \hbar 5 can be used to calculate the R_{IIM} value for a desired overcurrent threshold.

$$RILM (\Omega) = \frac{4834}{II.IM (A)}$$
 (5)

备注

- The TPS259480x/2x variants allow a maximum transient load current up to 2 × I_{LIM} for the ITIMER duration. The TPS259481x variants allow a maximum transient load current up to I_{FFT} for the ITIMER duration.
- 2. Leaving the ILM pin Open sets the current limit to zero and results in the part entering current limit or performing a fast-trip with the slightest amount of loading at the output.
- 3. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
- 4. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There's a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using 方程式 6.

CITIMER (nF) =
$$\frac{\text{tITIMER (ms)} \times \text{IITIMER (}\mu\text{A}\text{)}}{\Delta \text{VITIMER (}V\text{)}}$$
 (6)

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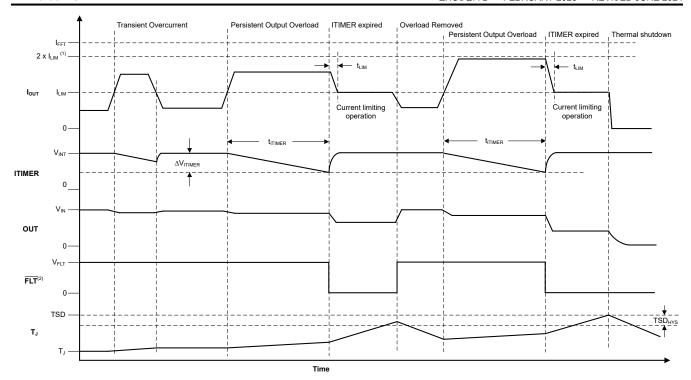


图 7-7. TPS25948xx Active Current Limit Response

备注

- 1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
- 2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
- Active current limiting based on R_{ILM} is active during startup. In case the startup current exceeds I_{LIM}, the device regulates the current to the set limit. However, during startup the current limit is engaged without waiting for the ITIMER delay.
- 4. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it will take lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage will drop resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. Once the part shuts down due to TSD fault, it would either stay latched off (TPS25948xL variants) or restart automatically after a fixed delay (TPS25948xA variants). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

7.3.3.3 Short-Circuit Protection

(1) Applicable only to TPS259480x/2x variants (2) Applicable only to TPS259480x variants

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. For the TPS259480x/2x variants, the internal fast-trip comparator employs a scalable threshold ($I_{SC} = 2 \times I_{LIM}$). This enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FFT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the maximum

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Applicable only to TPS259480x/2x variants



recommended user adjustable scalable fast-trip threshold. The TPS259481x variants employ only the fixed fast-trip threshold. Once the current exceeds I_{SC} or I_{FFT} , the HFET is turned off completely within t_{SC} or t_{FT} . Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30 μ s) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device will stay in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See Overtemperature Protection (OTP) section for details on the device response to overtemperature.

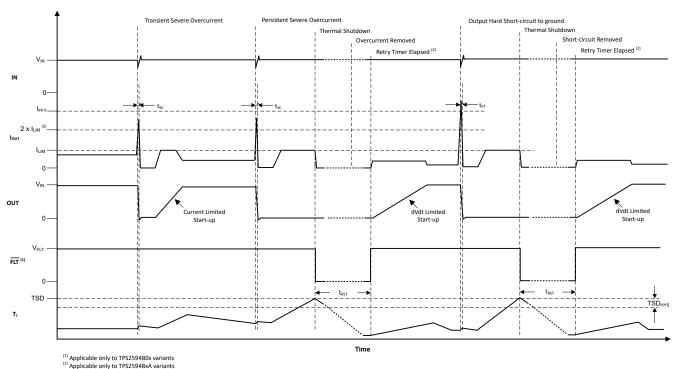


图 7-8. TPS259480x/2x Short-Circuit Response

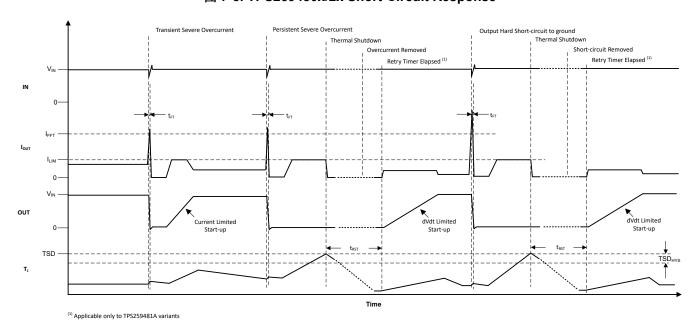
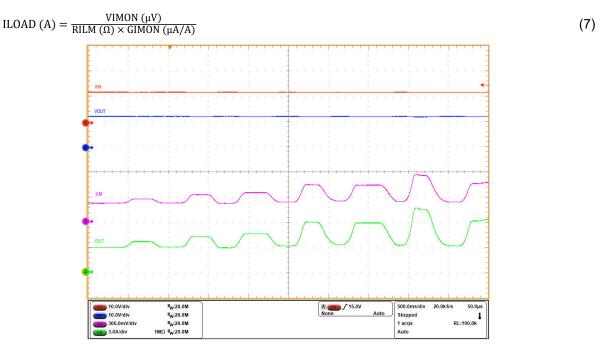


图 7-9. TPS259481x Short-Circuit Response

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7.3.4 Analog Load Current Monitor

The TPS25948xx allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{II M}) across the R_{II M} to get a measure of the output load current.



 V_{IN} = 12 V, C_{OUT} = 220 μ F, R_{ILM} = 536 Ω , I_{OUT} varied dynamically between 3 A and 8 A

图 7-10. Analog Load Current Monitor Response

备注

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

7.3.5 Reverse Current Protection

The TPS25948xx functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at V_{FWD}. This closed loop regulation scheme (linear ORing control) enables graceful turn off of the MOSFET during a reverse current event and ensures there's almost no DC reverse current flow.

The device also uses a conventional comparator (V_{REVTH}) based reverse blocking mechanism to provide fast response (t_{RCB}) to transient reverse currents. Once the device enters reverse current blocking condition, it waits for the (V_{IN} - V_{OUT}) forward drop to exceed the V_{FWDTH} before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysterisis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (t_{SWRCB}). This ensures minimum supply droop which is helpful in applications such as supply MUXing/ORing and USB Fast Role Swap (FRS).

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28



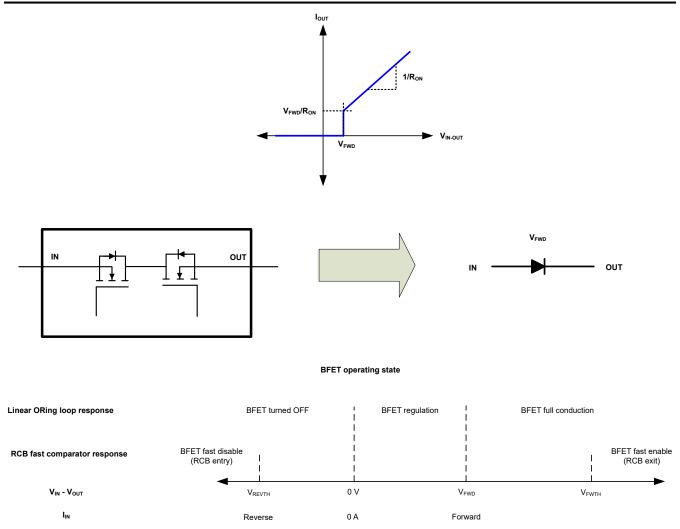


图 7-11. Reverse Current Blocking Response

The following waveforms illustrate the reverse current blocking performance in various scenarios.

During fast voltage step at output (e.g. hot-plug), the fast comparator based reverse blocking mechanism ensures minimum jump or glitch on the input rail.

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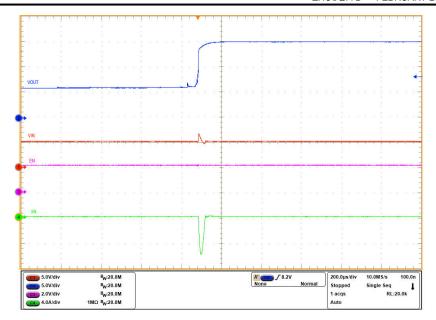


图 7-12. Reverse Current Blocking Performance During Fast Voltage Step at Output

During slow voltage ramp at output, the linear ORing based reverse blocking mechanism ensures there is almost no DC current flow from OUT to IN, thereby avoiding input rail from getting slowly charged up to output voltage.

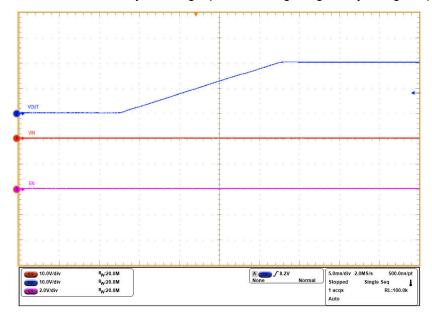


图 7-13. Reverse Current Blocking Performance During Slow Voltage Ramp at Output

When the input supply droops or gets disconnected while the output storage element (bulk capacitor or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum holdup time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

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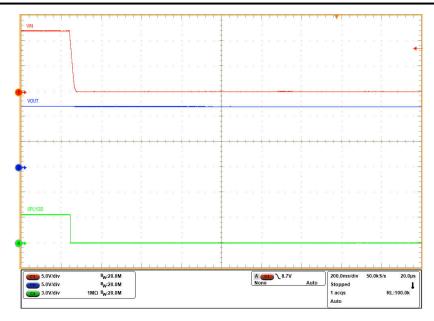


图 7-14. Reverse Current Blocking Performance During Input Supply Failure

The TPS259481x/2x variants provide the option of disabling the reverse current blocking scheme using the RCBCTRL pin. Leaving the RCBCTRL pin floating or pulling it high enables the reverse current blocking during steady-state, while pulling the pin low disables it.

备注

RCBCTRL pin controls the reverse current blocking mechanism only during steady-state. It has no effect during disabled or fault state where the reverse current blocking is always active.

7.3.6 Overtemperature Protection (OTP)

The TPS25948xx monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device will not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD - TSD_{HYS}).

When the TPS25948xL (latch-off variant) detects thermal overload, it will be shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS25948xA (auto-retry variant) detects thermal overload, it will remain off until it has cooled down by TSD_{HYS} . Thereafter, it will remain off for an additional delay of t_{RST} after which it will automatically retry to turn on if it is still enabled.

| Device | Enter TSD | Exit TSD |
|----------------------------|-----------------------|--|
| TPS25948xL (Latch-Off) | T _J ≥ TSD | $\rm T_J < TSD - TSD_{HYS}$ $\rm V_{IN}$ cycled to 0 V and then above $\rm V_{UVP(R)}$ OR EN/UVLO toggled below $\rm V_{SD(F)}$ |
| TPS25948xA (Auto-Retry) | $T_{J} \geqslant TSD$ | $\begin{split} & \text{T}_{\text{J}} < \text{TSD } - \text{TSD}_{\text{HYS}} \\ & \text{V}_{\text{IN}} \text{ cycled to 0 V and then above V}_{\text{UVP}(R)} \text{ OR EN/UVLO} \\ & \text{toggled below V}_{\text{SD}(F)} \text{ OR t}_{\text{RST}} \text{ timer expired} \end{split}$ |

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表 7-1. Thermal Shutdown

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7.3.7 Fault Response and Indication (FLT)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication (FLT) pin is available on the TPS259480x variants.

表 7-2. Fault Summary

| Event | Protection Response | Fault Latched Internally | FLT Pin Status (1) | FLT Assertion Delay ⁽¹⁾ |
|---|--|--------------------------|--------------------|------------------------------------|
| Overtemperature | Shutdown | Υ | L | |
| Undervoltage (UVP or UVLO) Shutdown | | N | Н | |
| Input Overvoltage | Shutdown | N | Н | |
| | None | N | н | |
| Persistent Overcurrent | Current Limit | N | L | t _{ITIMER} |
| Output Short-Circuit to GND | Circuit Breaker followed by Current Limit | N | Н | |
| ILM Pin Open (During Steady State) | Shutdown | N | Н | |
| ILM Pin Shorted to GND | Shutdown | Υ | L | |
| Reverse Current ((V _{OUT} - V _{IN}) > V _{REVTH}) | Reverse Current Blocking | N | н | |

Applicable to TPS259480x variants only.

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below $V_{SD(F)}$. This also releases the FLT pin pull-down for the TPS259480x variants and resets the t_{RST} timer for the TPS25948xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This is true for both TPS25948xL (latch-off) and TPS25948xA (auto-retry) variants.

For TPS25948xA (auto-retry) variants, on expiry of the t_{RST} timer after a fault, the device restarts automatically and the FLT pin is de-asserted (TPS259480A variant).

7.3.8 Supply Good Indication (SPLYGD/SPLYGD)

The TPS25948xx provides a digital output (SPLYGD/SPLYGD) which is asserted to indicate when the priority input supply is in a valid range (above UVP/UVLO and below OVLO thresholds) and the device has successfully completed its inrush sequence. The SPLYGD/SPLYGD pin is an open-drain signal which needs to be pulled up to an external supply. For the TPS259480x/2x variants, SPLYGD is an active high output. For the TPS259481x variant, SPLYGD is an active low output.

After power up, SPLYGD/SPLYGD pin is de-asserted initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the FET gate voltage has reached the full overdrive indicating that the inrush sequence is complete and device is capable of delivering full power, the SPLYGD/SPLYGD pin is asserted. Thereafter, the SPLYGD/SPLYGD pin is de-asserted only if the input supply becomes invalid (below UVP/UVLO or above OVLO thresholds). No load side events/faults have any control over the SPLYGD/SPLYGD de-assertion.

This pin is used to control the auxiliary channel when 2 TPS25948xx devices are connected in a priority power MUX configuration. It can also be used as a supply valid status indication to the downstream load or system supervisor.

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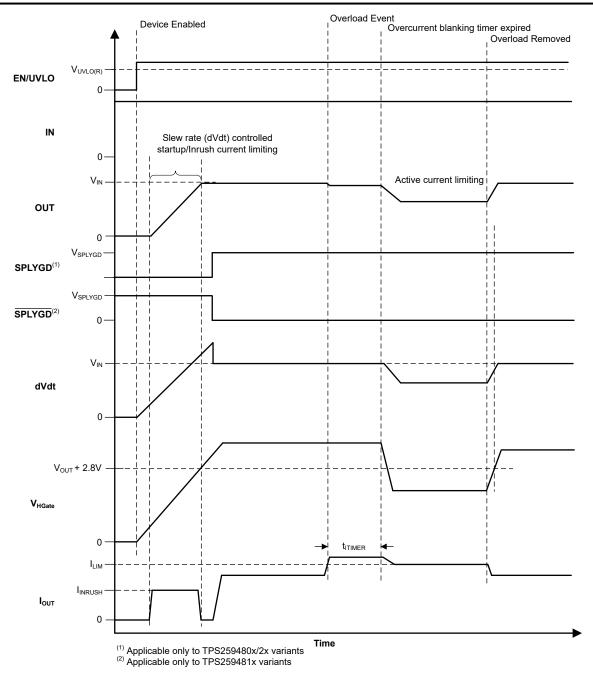


图 7-15. TPS25948xx SPLYGD Behavior

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32

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表 7-3. TPS25948xx SPLYGD/SPLYGD Indication Summary

| Event/Condition | SPLYGD Pin ⁽¹⁾ | SPLYGD Pin ⁽²⁾ |
|---|---------------------------|---------------------------|
| Supply Brownout (UVP) | L | L |
| Shutdown (EN < V _{SD}) | L | L |
| Undervoltage (UVLO) | L | Н |
| Overvoltage (OVLO) | L | Н |
| Inrush | L | Н |
| Steady State | Н | L |
| Overcurrent | Н | L |
| Short-Circuit | Н | L |
| ILM Pin Open | Н | L |
| ILM Pin Shorted to GND | Н | L |
| Reverse current ((V _{OUT} - V _{IN}) > V _{REVTH}) | Н | L |
| Overtemperature | Н | L |

- (1) Applicable only to TPS259480x/2x variants.
- (2) Applicable only to TPS259481x variants.

When there is no supply to the device, the SPLYGD pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the SPLYGD pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition. This also ensures that the auxiliary channel is not turned off inadvertently in a priority power MUX configuration.

7.4 Device Functional Modes

表 7-4. TPS259481x/2x Reverse Current Blocking Operation

| RCBCTRL Pin Connection | Reverse Current Blocking in Steady-State | | |
|------------------------|--|--|--|
| Low | Disabled | | |
| Open or High | Enabled | | |

Product Folder Links: TPS25948

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English Data Sheet: SLVSGT9



8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25948x is a 3.5 V to 23 V, 8-A eFuse that is typically used for power rail protection applications. It operates from 3.5 V to 23 V with adjustable overvoltage and undervoltage protection. It provides ability to control inrush current and protection against reverse current conditions. It can be used in a variety of systems such as adapter or charger input protection, USB PD protection in smartphone, tablet, PC, notebook, monitor, dock, server and PC motherboard, add-on cards, enterprise storage - RAID/HBA/SAN/eSSD, power MUXing/ORing. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool TPS25948x Design Calculator is available in the web product folder.

8.2 Single Device, Self-Controlled

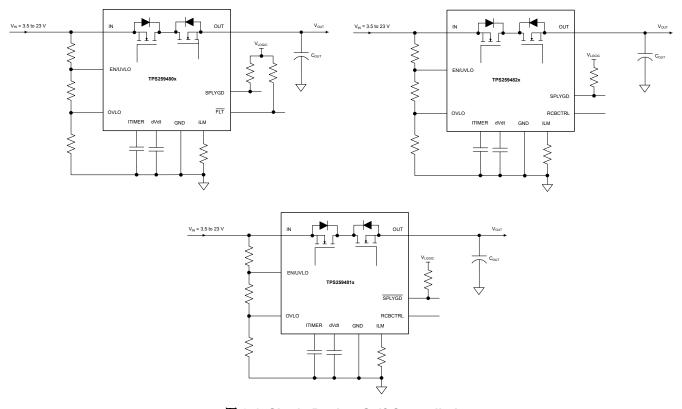


图 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

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ILM pin can be connected to the MCU ADC input for current monitoring purpose.

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备注

It is recommended to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation.

8.3 Typical Application

Smartphones come equipped with USB OTG functionality that allows their USB port to be used not only for charging the phone battery but also allow the smartphone to act as a USB host and deliver power to external accessories such as headphones, pen drives, and so forth. Some smartphones also support a wireless charging path which can also be used to wirelessly share power to other devices. TPS259482x can be used as a bidirectional power switch in such applications as shown in 88.3. For the USB power path, when an external charger is connected at the port, TPS259482x provides a conduction path from IN pin to OUT pin and the battery charger IC is configured to charge the battery and also power the internal circuits. TPS259482x also provides overvoltage and overcurrent protection in this case. In another use case scenario where an accessory such as headphone is connected to the USB port, the phone MCU detects this and the battery charger is configured in OTG boost mode to provide power from battery to the USB port. MCU will also pull down RCBCTRL pin to allow current flow from OUT pin to IN pin of TPS259482x and enables the TPS259482x and establishes a low impedance power path capable of delivering high power to the accessory. Similarly, the TPS259482x also provides controlled bi-directional power flow in the wireless charging and power share subsystem.

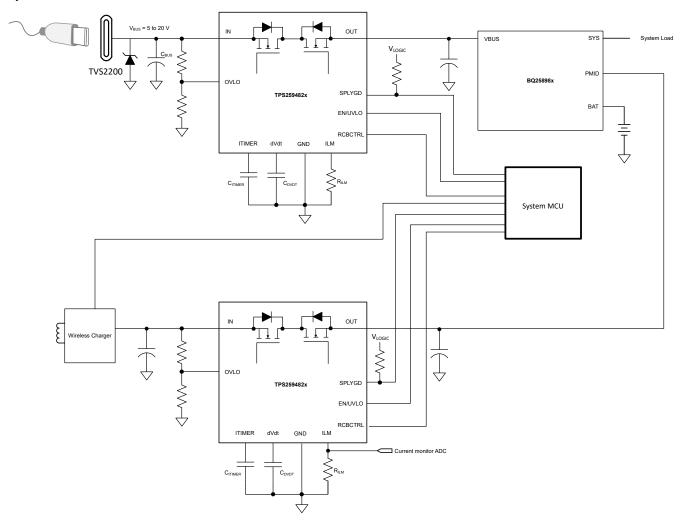
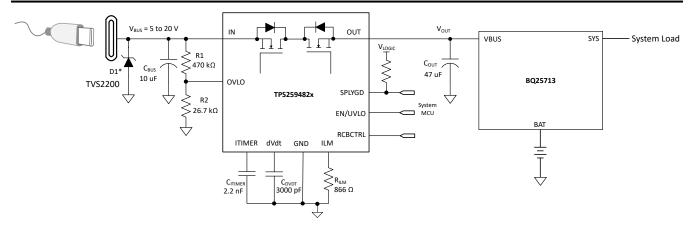


图 8-2. Smartphone Power Path Example

Product Folder Links: TPS25948





^{*} Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

图 8-3. USB On-The-Go Port Protection Design Example

8.3.1 Design Requirements

表 8-1. Design Parameters

| , , , , , , , , , , , , , , , , , , , | | | | | |
|---|----------------------|--|--|--|--|
| PARAMETER | VALUE | | | | |
| Bus voltage during charging (V _{IN}) | 20 V | | | | |
| Overvoltage protection threshold during charging (V _{IN(OV)}) | 22 V | | | | |
| Max continuous charging current | 5 A | | | | |
| Load transient blanking interval during charging (t _{ITIMER}) | 2 ms | | | | |
| Output capacitance (C _{OUT}) | 47 μ F | | | | |
| Output rise time (t _R) | 12 ms | | | | |
| Overcurrent threshold (I _{LIM}) during charging | 5.5 A | | | | |

8.3.2 Detailed Design Procedure

8.3.2.1 Setting Overvoltage Threshold

The supply overvoltage threshold is set using the resistors, R1 and R2, whose values can be calculated as:

$$VIN(OV) = \frac{VOV(R) \times (R1 + R2)}{R2}$$
(8)

Where $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 leak the current from input supply V_{IN} , these resistors must be selected based on the acceptable leakage current from input power supply V_{IN} . The current drawn by R1, R2 from the power supply is IR12 = V_{IN} / (R1 + R2). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR12, must be chosen to be 20 times greater than the leakage current expected on the OVLO pin.

From the device electrical specifications, OVLO leakage current is 0.1 μ A (maximum), $V_{OV(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 22 V. To solve the equation, first choose the value of R1 = 470 k Ω and use the above equation to solve for R2 = 27.11 k Ω .

Using the closest standard 1% resistor values, we get R1 = 470 k Ω , R2 = 26.7 k Ω .

8.3.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of

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magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR (V/ms) = \frac{VIN (V)}{tR (ms)} = \frac{20 V}{12 ms} = 1.67 V/ms$$
 (9)

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$CdVdt (pF) = \frac{5000}{SR (V/ms)} = \frac{5000}{1.67} = 2994 pF$$
 (10)

Choose the nearest standard capacitor value as 3000 pF.

For this slew rate, the inrush current can be calculated as:

IINRUSH (mA) = SR (V/ms) x COUT (
$$\mu$$
F) = 1.67 x 47 = 79 mA (11)

The average power dissipation inside the part during inrush can be calculated as:

PDINRUSH (W) =
$$\frac{\text{IINRUSH (A)} \times \text{VIN (V)}}{2} = \frac{0.079 \times 20}{2} = 0.8 \text{ W}$$
 (12)

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 8-4 shows the thermal shutdown limit, for 0.8 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 12 ms. Therefore, it is safe to use 12 ms as the startup time for this application.

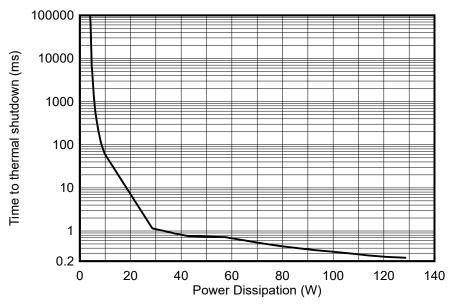


图 8-4. Thermal Shut-Down Plot During Inrush

8.3.2.3 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection threshold can be set using the R_{ILM} resistor whose value can be calculated as:

RILM (
$$\Omega$$
) = $\frac{4834}{\text{ILIM (A)}} = \frac{4834}{5.5 \text{ A}} = 879 \Omega$ (13)

Choose nearest 1% standard resistor value as 866 Ω .

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38



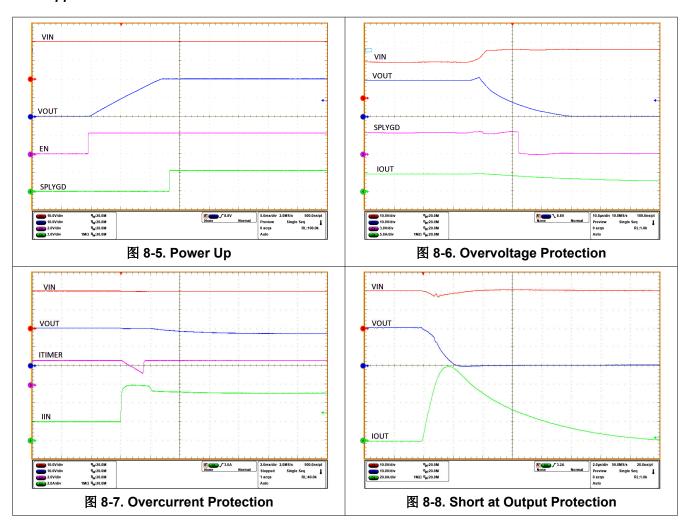
8.3.2.4 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

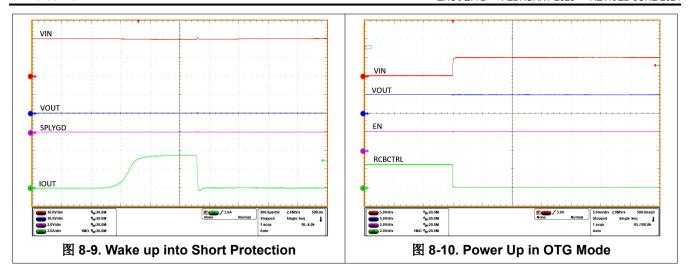
CITIMER (nF) =
$$\frac{\text{tITIMER (ms)} \times \text{IITIMER (}\mu\text{A}\text{)}}{\Delta \text{ VITIMER (}V\text{)}} = \frac{2 \times 1.9}{1.51} = 2.51 \text{ nF}$$
 (14)

Choose nearest standard capacitor value as 2.2 nF.

8.3.3 Application Curves



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8.4 Active ORing

A typical redundant power supply configuration is shown in 88-11 below. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The TPS25948xx with integrated, low-ohmic, back-to-back FETs provide a simple and efficient solution. 88-11 below shows the Active ORing implementation using TPS259480x devices.

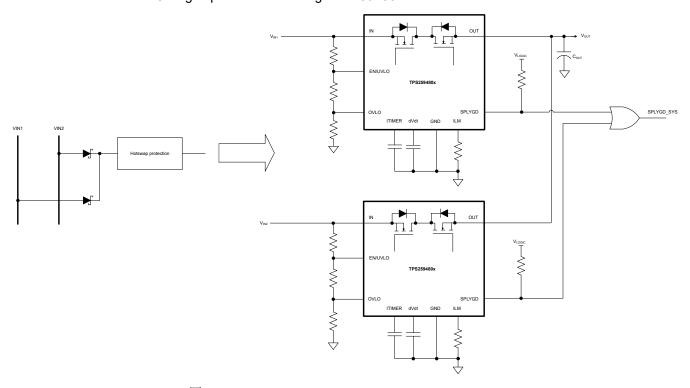
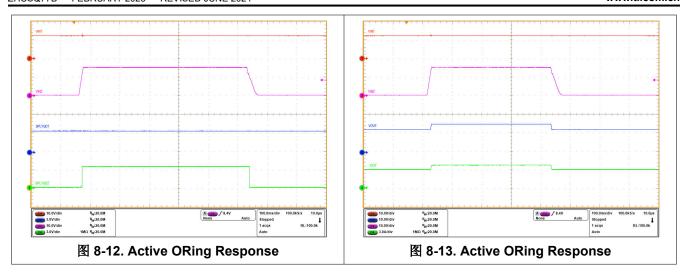


图 8-11. Two Devices, Active ORing Configuration

The linear ORing mechanism in TPS25948xx ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveform illustrates the active ORing behavior when the supply rails are being ramped up sequentially.

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When the bus voltages (IN1 and IN2) are matched, device in each path sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to supply ORing, the devices protect the system from overvoltage, excessive inrush current, overload and short-circuit faults at all times.

备注

ORing can be done either between two similar rails or between dissimilar rails. For ORing cases with skewed voltage combinations, the dVdt pin capacitor rating should be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

8.5 Priority Power MUXing

Applications having two energy sources such as PCIe cards, Tablets and Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal battery back-up power. These applications demand for switchover from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS25948xx devices provide a simple solution for priority power multiplexing needs.

8-14 shows a typical priority power multiplexing implementation using TPS259480x devices. When primary (priority) power source (IN1) is present and within the valid range (not in UV/OV condition), the primary path device path powers the OUT bus irrespective of whether auxiliary supply voltage (V_{IN2}) is greater than, equal to or less than primary supply voltage (V_{IN1}). The device in auxiliary path is held in off condition by forcing its OVLO pin to high using the SPLYGD signal from the primary path device.

Once the primary supply voltage falls outside the user-defined valid operating range (UV/OV condition), the primary path device de-asserts the SPLYGD which signals the auxiliary path device to turn on and the system starts operating from the auxiliary supply. During this transition, the auxiliary path device bypasses its dVdt limited startup and performs a fast recovery to start delivering power within t_{SWOV} .

When the primary supply is restored, the primary path device turns on fully at a defined slew rate and then asserts its SPLYGD pin high to turn the auxiliary path device off, allowing a seamless transition from auxiliary to the primary supply with minimal output voltage droop and with no shoot-through current.

A key consideration in power MUXing applications is the minimum voltage the output bus droops to during the switchover from one supply to another. This in turn depends on multiple factors including the output load current ($I_{I,OAD}$), output bus hold-up capacitance (C_{OUT}) and switchover time (I_{SW}).

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While switching from primary supply (V_{IN1}) to auxiliary supply (V_{IN2}) , the minimum bus voltage can be calculated using 方程式 15. Here, the switchover time (t_{SW}) is equal to the fast OVLO recovery time (t_{SWOV}) taken by the TPS259480x variants to turn on fully and start delivering current to the load.

VOUT,min (V) = min (VIN1, VIN2) -
$$\frac{\text{tSW }(\mu s) \times \text{ILOAD }(A)}{\text{COUT }(\mu F)}$$
 (15)

While switching from auxiliary supply (V_{IN2}) to primary supply (V_{IN1}) , the minimum bus voltage can be calculated using 方程式 16. Here the maximum switchover time is equal to the RCB recovery time (t_{SWRCB}) , depending on whether V_{IN1} is equal to or lower than V_{IN2} to start with.

VOUT,min (V) = min (VIN1, VIN2) - VFWDTH (V) -
$$\frac{\text{tSWRCB }(\mu s) \times \text{ILOAD }(A)}{\text{COUT }(\mu F)}$$
 (16)

The SPLYGD pins of the devices can be used as a digital indication to identify which of the 2 supplies is active and delivering power to the load.

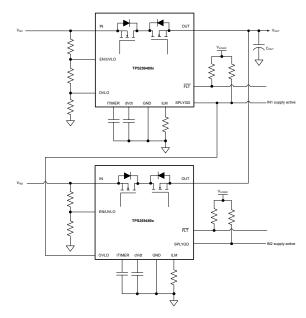


图 8-14. Priority Power MUXing With 2 × TPS259480x - Option 1

This configuration provides the most compact priority power MUXing solution with multiple benefits, including active current limit protection on both channels as well as overvoltage protection on primary channel. It also provides the fastest switchover time from primary to auxiliary, but at the cost of a slightly increased quiescent current on the auxiliary path while primary path is active. Also, it uses the fewest external components, but at the cost of bypassing overvoltage protection on auxiliary channel.

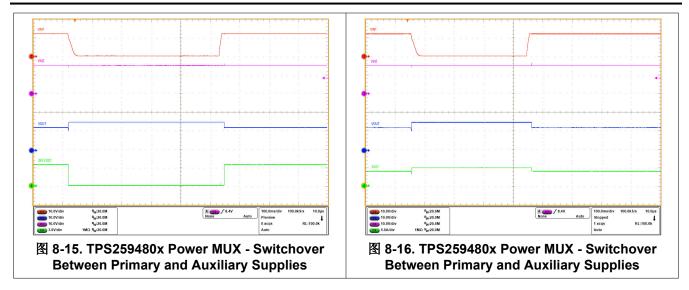
The following waveforms illustrate the TPS259480x performance in a priority power MUXing configuration.

English Data Sheet: SLVSGT9

41

Product Folder Links: TPS25948





ere is a possible variation to the above configuration in case overvoltage protection is needed on both channels. This needs an additional signal N-FET to drive the OVLO pin of the auxiliary path device as shown in 图 8-17. The switchover times are similar to the previous configuration.

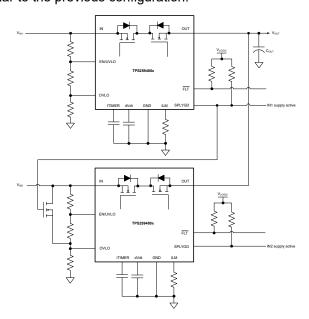


图 8-17. Priority Power MUXing With 2 × TPS259480x - Option 2

Another variation of the previous configuration ensures minimum quiescent current on the auxiliary channel while primary channel is active, but at the cost of additional N-FET to drive the EN/UVLO pin of auxiliary path device as shown in 88.18. At the same time, it has a higher switchover delay from primary to auxiliary supply as compared to the previous configuration.

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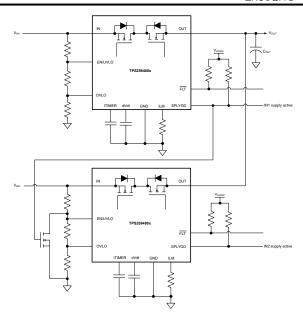


图 8-18. Priority Power MUXing With 2 × TPS259480x - Option 3

While switching from a higher supply rail to lower supply rail, the minimum bus voltage can be calculated using 方程式 17. Here, the switchover time is equal to the time taken by the device to come out of reverse current blocking state (t_{SWRCB}).

VOUT,min (V) = min (VIN1, VIN2) - VFWDTH (V) -
$$\frac{\text{tSWRCB }(\mu s) \times \text{ILOAD }(A)}{\text{COUT }(\mu F)}$$
 (17)

While switching from a lower supply rail to higher supply rail, the minimum bus voltage can be calculated using 方程式 18. Here, the switchover time (t_{SW}) is the time taken by the device to turn on fully and start delivering current to the load, which is equal to the device turn-on time (t_{ON}) , which in turn includes the turn-on delay $(t_{D,ON})$ and rise time (t_R) determined by the dVdt capacitor (C_{dVdt}) and bus voltage.

VOUT,min (V) = min (VIN1, VIN2) -
$$\frac{\text{tSW }(\mu s) \times \text{ILOAD }(A)}{\text{COUT }(\mu F)}$$
 (18)

备注

- 1. Power MUXing can be done either between two similar rails (such as 12-V Primary and 12-V Aux, 3.3-V Primary and 3.3-V Aux) or between dissimilar rails (such as 12-V Primary and 5-V Aux or vice versa).
- 2. For power MUXing cases with skewed voltage combinations, care must be taken to design circuit components on EN/OVLO pins for the lower voltage channel devices such that the absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating should be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

8.6 Parallel Operation

Applications which need higher steady current can use 2 or more TPS25948x devices connected in parallel as shown in 88-19. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the SPLYGD signal of the first device. Once the inrush sequence is complete, the first device asserts its SPLYGD pin high and turns on the second device. The second device asserts its SPLYGD signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

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Once in steady state, both devices share current nearly equally. There could be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

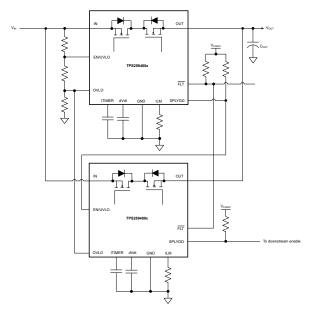
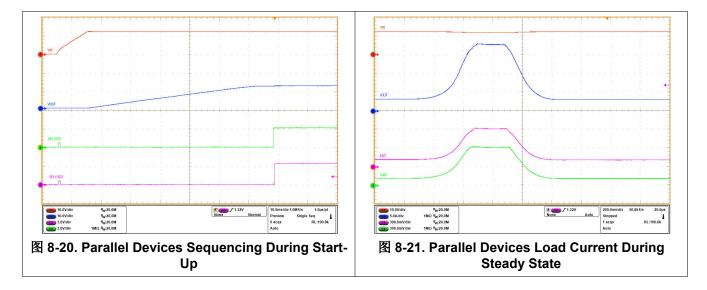


图 8-19. Two Devices Connected in Parallel for Higher Steady State Current Capability

The following waveforms illustrate the behavior of parallel configuration during start-up as well as during steady state.



8.7 USB PD Port Protection

End equipments like PC, Notebooks, Docking Stations, Monitors etc.. have USB PD ports which can be configured as DFP (Source), UFP (Sink) or DRP (Source+Sink). TPS25948xx can be used to as a fully integrated power path solution for USB PD ports as shown in

8 8-22 below.

TPS25948xx provides all the basic protection functions needed on the USB power path e.g. overvoltage, overcurrent and short-circuit protection along with monitoring and control. The linear ORing mechanism in TPS25948xx ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

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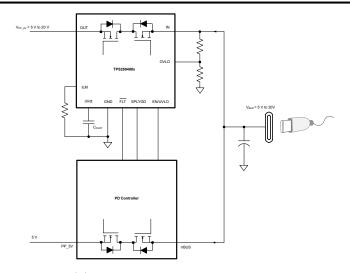


图 8-22. USB PD Port Protection

8.8 Power Supply Recommendations

The TPS25948x devices are designed for a supply voltage range of 3.5 V \leq V_{IN} or V_{OUT} \leq 23 V. An input ceramic bypass capacitor higher than 0.1 $\,\mu$ F is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.8.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- · Minimize lead length and inductance into and out of the device.
- · Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 μ F at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 μF to absorb the energy and dampen the transients. The
 capacitor voltage rating should be atleast twice the input supply voltage to be able to withstand the positive
 voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with the equation:

$$VSPIKE(ABSOLUTE) = VIN + ILOAD \times \sqrt{\frac{LIN}{CIN}}$$
(19)

where

- V_{IN} is the nominal supply voltage.
- I_{LOAD} is the load current.
- L_{IN} equals the effective inductance seen looking into the source.
- C_{IN} is the capacitance present at the input.
- Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients
 from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude
 of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive
 energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which
 can couple to the internal control circuits and cause unexpected behavior.
- For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there could be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. It's recommended to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in \(\begin{align*} \text{8-23}. \\ \end{align*}

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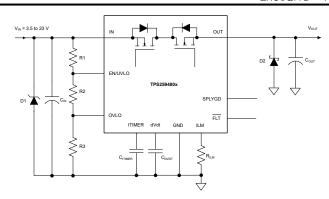


图 8-23. Circuit Implementation with Optional Protection Components

8.8.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- · Component selection
- · Output shorting method
- · Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.9 Layout

8.9.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. It's recommended to have a separate ground plane island for the eFuse. This plane doesn't carry any high currents and serves as a guiet ground reference for all the critical analog signals of the eFuse. The device ground plane should be connected to the system power ground plane using a star connection.
- The IN and OUT pads are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient accross the IN and OUT pads and distribute current unformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.

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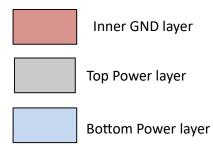


- Locate the following support components close to their connection pins:
 - $-R_{ILM}$
 - C_{dVdT}
 - C_{ITIMER}
 - Resistors for the EN/UVLO and OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace
 routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce
 parasitic effects on the current limit, overcurrent blanking interval and soft start timing. It's recommended to
 keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have
 any coupling to switching signals on the board.
- Since the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the
 device they are intended to protect. These protection devices must be routed with short traces to reduce
 inductance. For example, a protection Schottky diode is recommended to address negative transients due to
 switching of inductive loads. It's also recommended to add a ceramic decoupling capacitor of 1 μ F or greater
 between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to
 minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND
 terminal of the IC.

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8.9.2 Layout Example



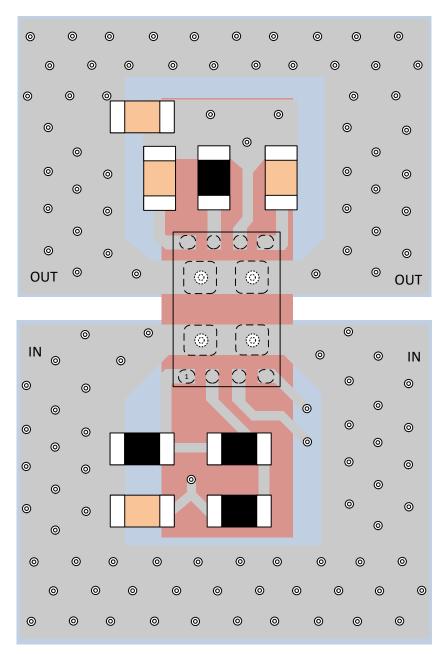


图 8-24. Layout Example

Product Folder Links: TPS25948



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- TPS25948EVM eFuse Evaluation Board
- TPS25948x Design Calculator
- · Application brief eFuses for USB Type-C protection

9.2 接收文档更新通知

要接收文档更新通知,请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

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链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范,并且不一定反映 TI 的观点;请参阅 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI术语表本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注:以前版本的页码可能与当前版本的页码不同

| С | hanges from Revision A (September 2023) to Revision B (June 2024) | Page |
|---|--|------|
| • | 向 <i>特性</i> 部分添加了"IEC 61000-4-5" | 1 |
| • | 删除了说明部分对反极性的引用 | 1 |
| • | Changed $V_{IN,MAX}$, – 40°C \leqslant T _J \leqslant 125°C from: V_{OUT} – 21V to: – 0.3V in the Absolute Maximum Ra section | - |
| • | Deleted $V_{IN,MAX}$, – 10°C \leq T _J \leq 125°C from the Absolute Maximum Ratings section | |
| С | hanges from Revision * (February 2023) to Revision A (September 2023) | Page |
| • | 将文档状态从 <i>预告信息</i> 更改为 <i>量产数据</i> | 1 |

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TPS25948

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www.ti.com 23-May-2025

PACKAGING INFORMATION

| Orderable part number | Status | Material type | Package Pins | Package qty Carrier | RoHS | Lead finish/ | MSL rating/ | Op temp (°C) | Part marking |
|-----------------------|--------|---------------|------------------|-----------------------|------|---------------|--------------------|--------------|--------------|
| | (1) | (2) | | | (3) | Ball material | Peak reflow | | (6) |
| | | | | | | (4) | (5) | | |
| TPS259480AYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259480A |
| TPS259480AYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259480A |
| TPS259480LYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259480L |
| TPS259480LYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259480L |
| TPS259481AYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259481A |
| TPS259481AYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259481A |
| TPS259481LYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259481L |
| TPS259481LYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259481L |
| TPS259482AYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259482A |
| TPS259482AYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259482A |
| TPS259482LYWPR | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259482L |
| TPS259482LYWPR.A | Active | Production | DSBGA (YWP) 12 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | 259482L |

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

| A0 | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

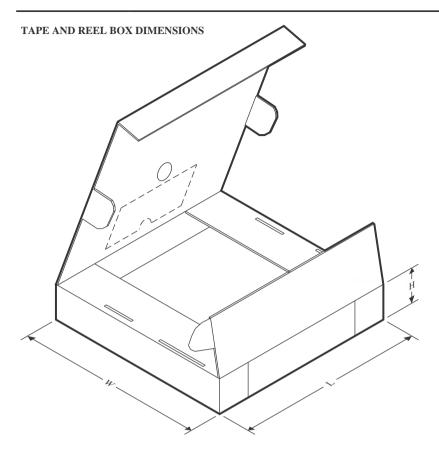


*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| TPS259480AYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS259480LYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS259481AYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS259481LYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS259482AYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS259482LYWPR | DSBGA | YWP | 12 | 3000 | 180.0 | 8.4 | 1.88 | 2.59 | 0.53 | 4.0 | 8.0 | Q2 |



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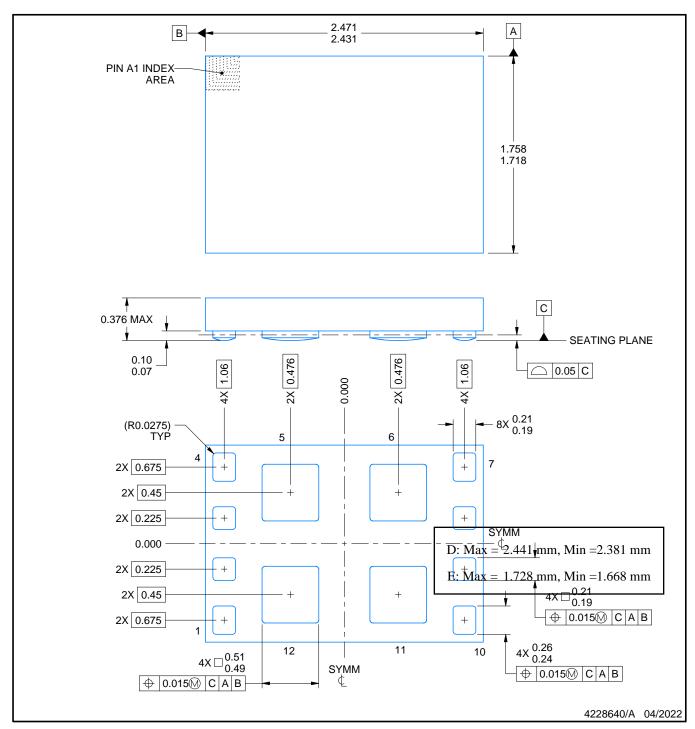


*All dimensions are nominal

| Device | Device Package Type | | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|---------------------|-----|------|------|-------------|------------|-------------|
| TPS259480AYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS259480LYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS259481AYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS259481LYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS259482AYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS259482LYWPR | DSBGA | YWP | 12 | 3000 | 182.0 | 182.0 | 20.0 |



POWER CHIP SCALE PACKAGE

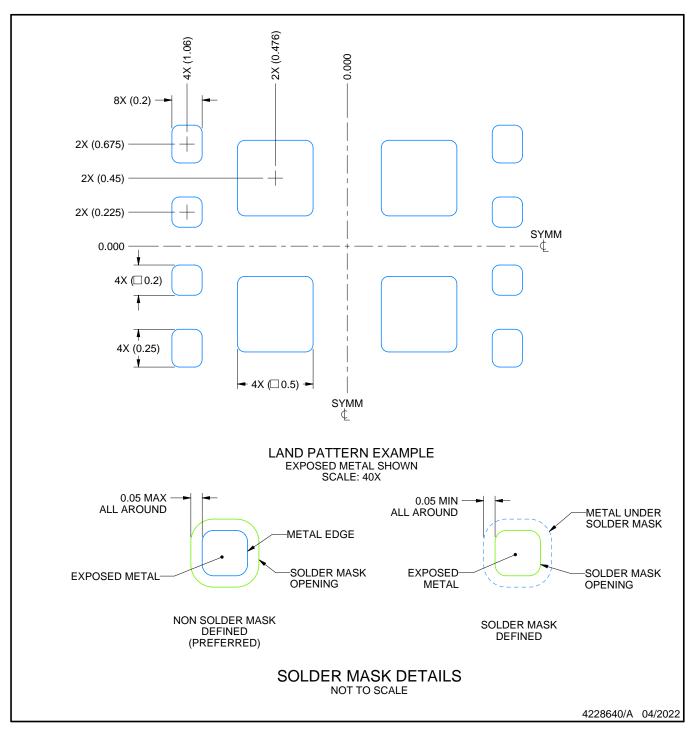


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



POWER CHIP SCALE PACKAGE

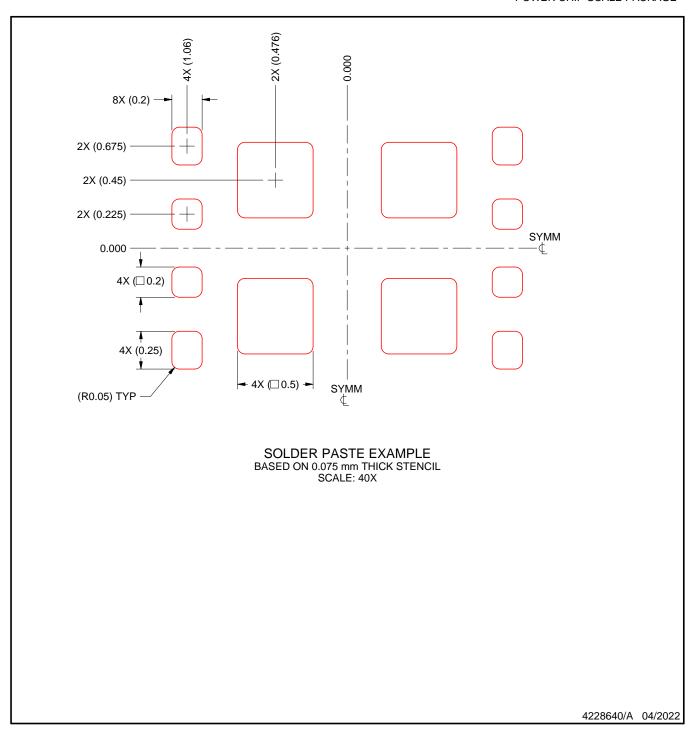


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



POWER CHIP SCALE PACKAGE



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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