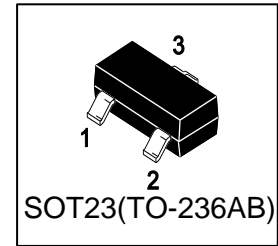


LN2292LT1G

100V N-Channel Enhancement-Mode MOSFET

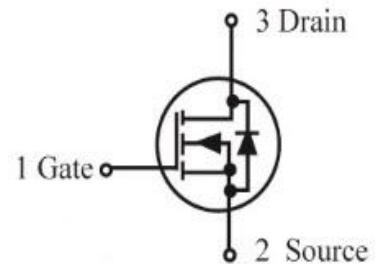
1. FEATURES

- $V_{DS} = 100V$
- $R_{DS(ON)} \leq 200 \text{ m}\Omega @ V_{GS} = 10V, I_D = 3A$
- $R_{DS(ON)} \leq 260 \text{ m}\Omega @ V_{GS} = 4.5V, I_D = 1A$
- Super high density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2292LT1G	N2L	3000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	V_{DS}	100	V
Gate–to–Source Voltage – Continuous	V_{GS}	± 20	V
Drain Current			
– Continuous $T_a = 25^\circ\text{C}$ (Note 1)	I_D	1.6	A
– Pulsed	I_{DM}	6.4	
– Continuous $T_a = 25^\circ\text{C}$ (Note 2)	I_D	1.1	A
– Pulsed	I_{DM}	4.5	
Avalanche Current	I_{AS}	9.6	A
Avalanche energy $L=0.1\text{mH}$	E_{AS}	4.6	mJ

5. THERMAL CHARACTERISTICS

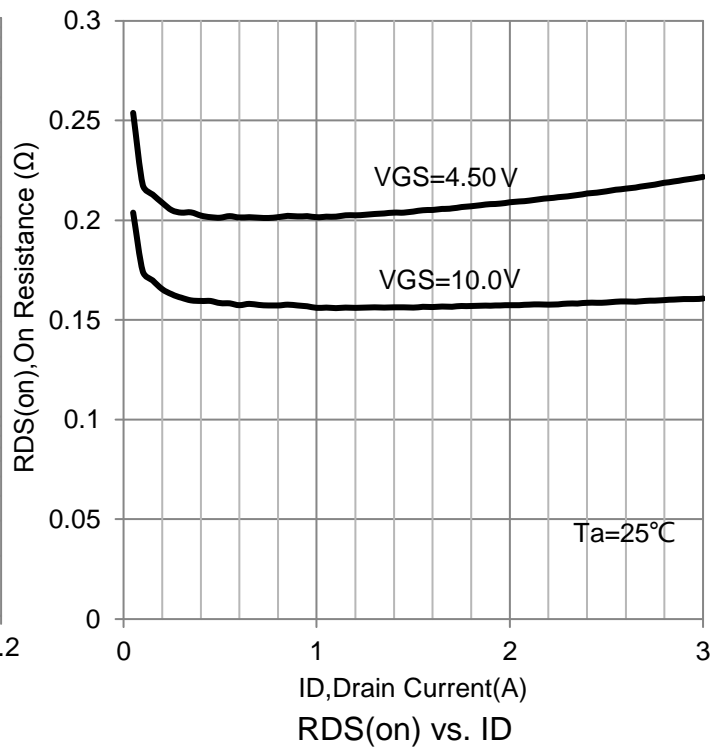
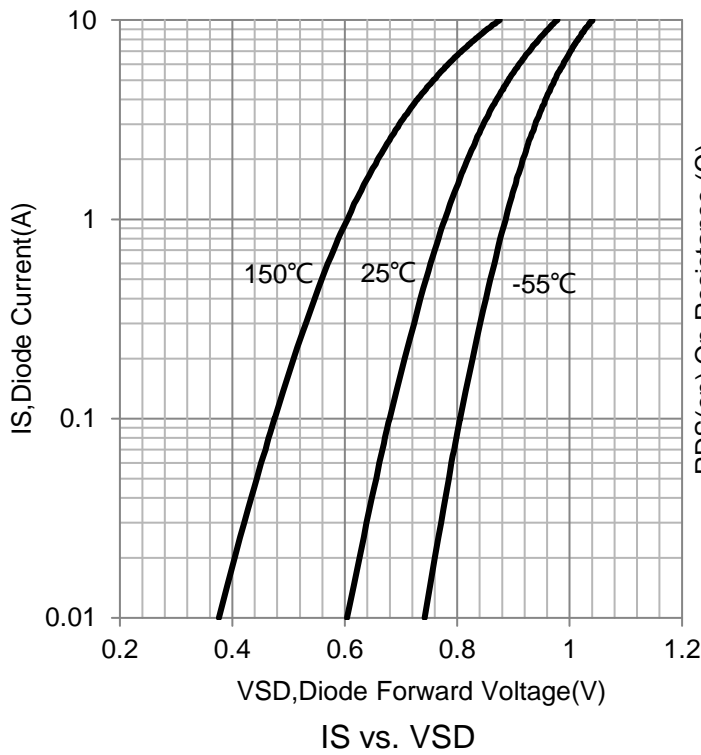
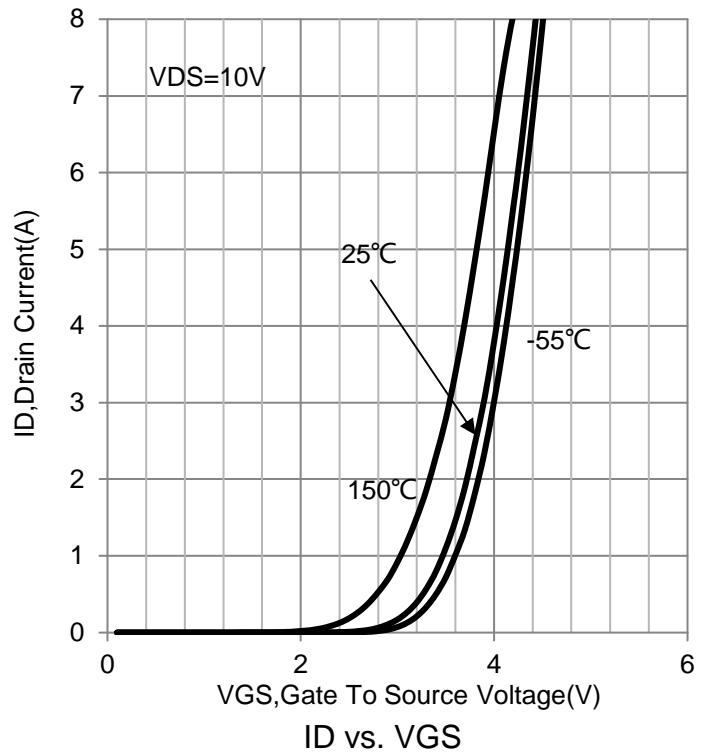
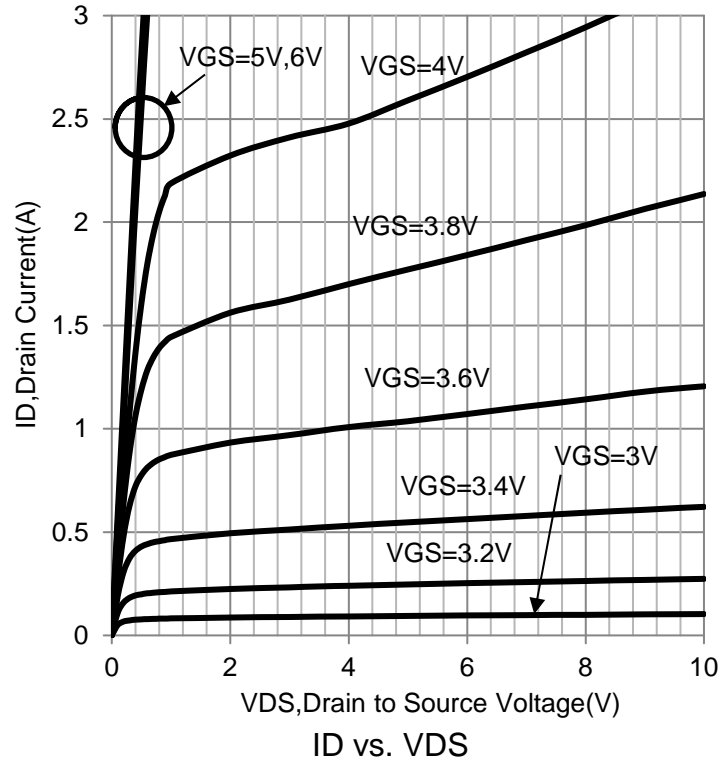
Parameter	Symbol	Limits	Unit
Maximum Power Dissipation(Note 1)	P_D	1.25	W
Maximum Power Dissipation(Note 2)	P_D	0.6	W
Thermal Resistance,			
Junction–to–Ambient(Note 1)	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
Junction–to–Ambient(Note 2)	$R_{\theta JA}$	205	
Junction–to–Case	$R_{\theta JC}$	25	
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

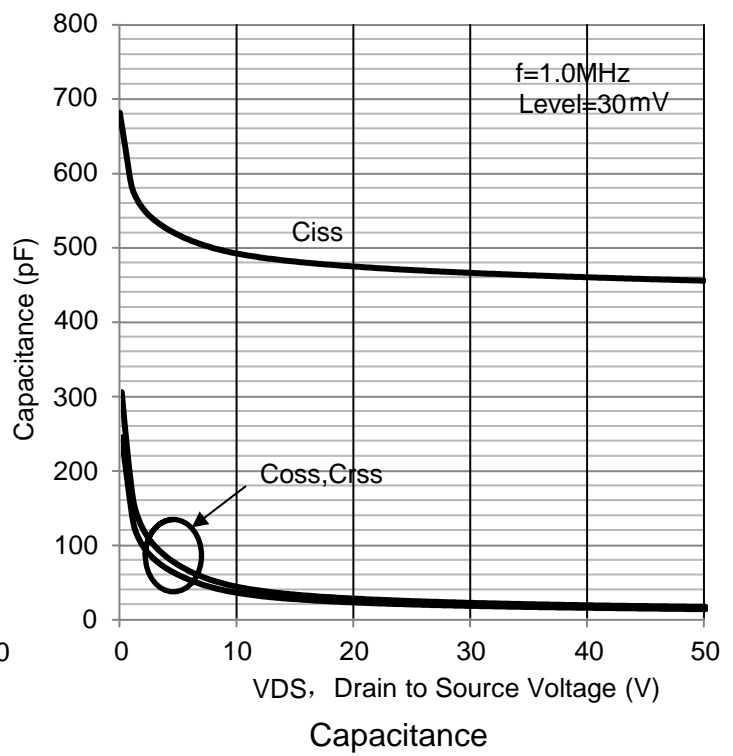
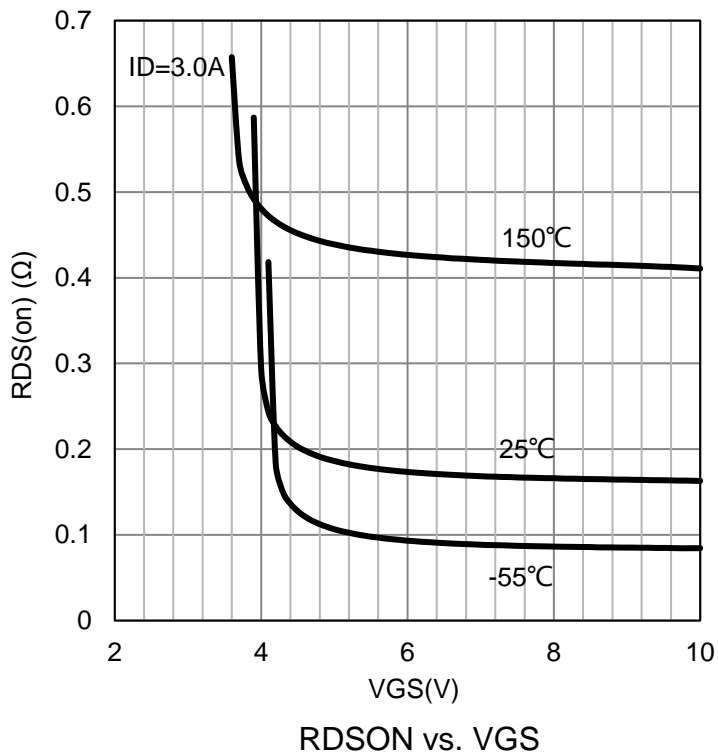
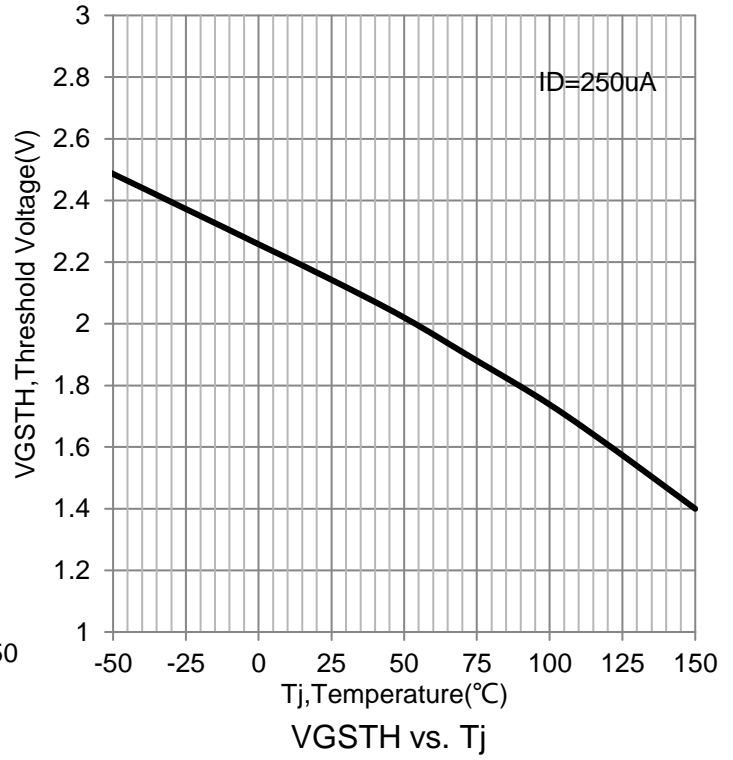
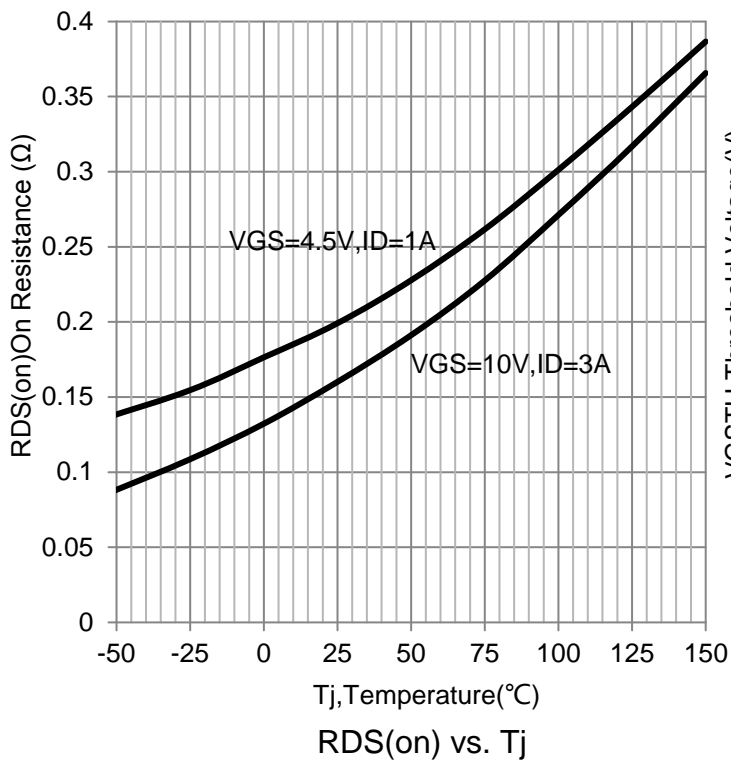
- 1.Surface–mounted on FR4 board using 1 sq–in pad, 2 oz Cu.
- 2.Surface mounted on FR4 board using the minimum recommended pad size.

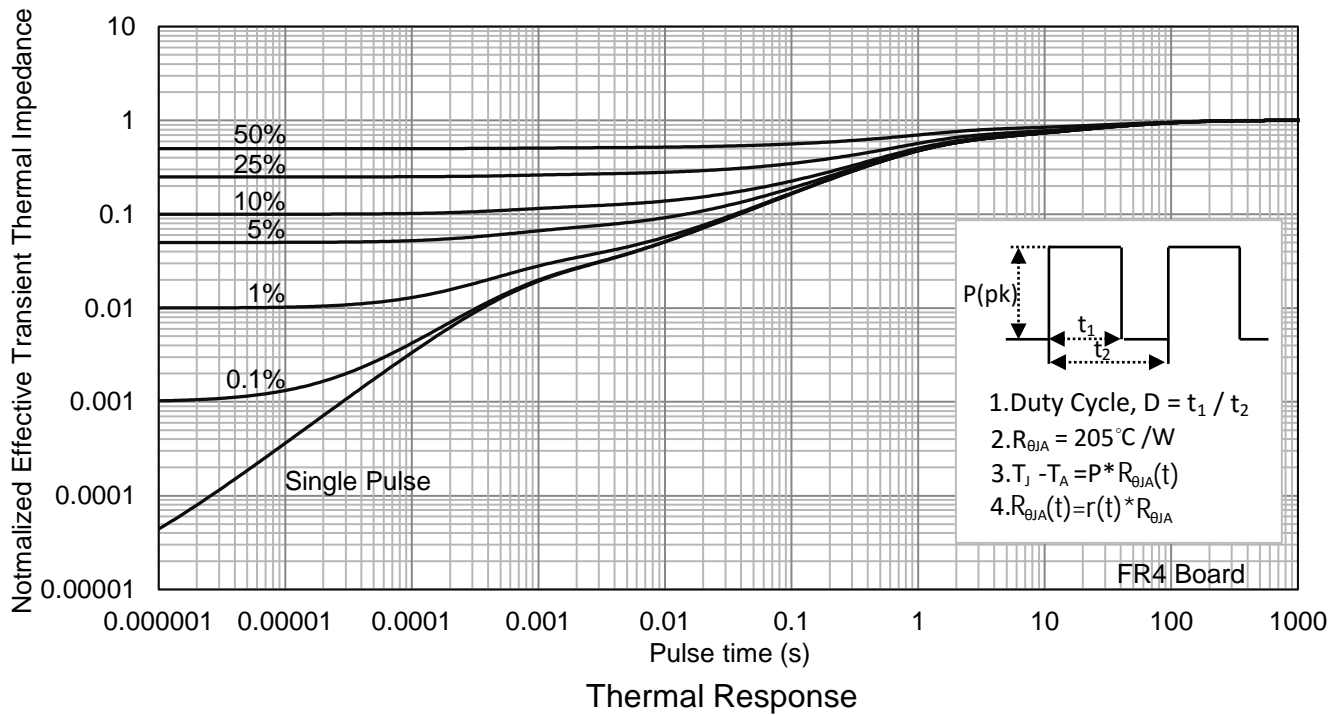
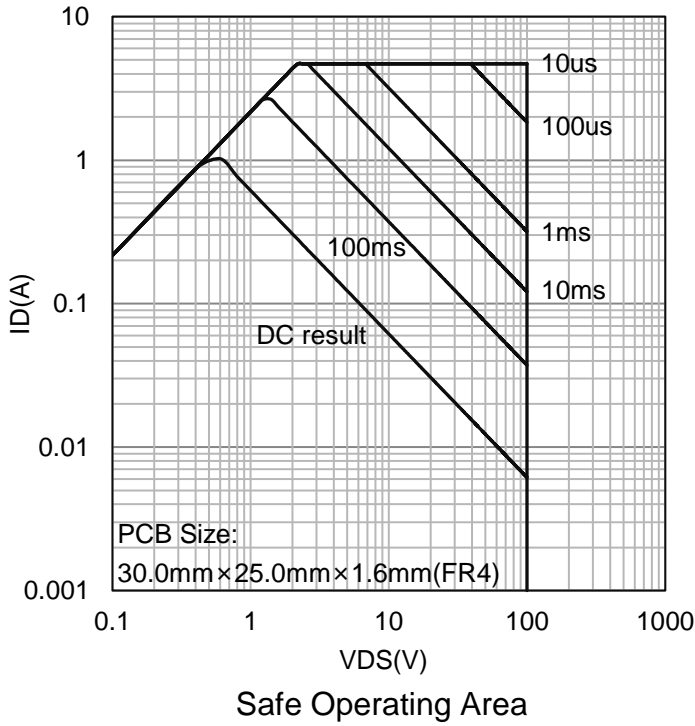
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

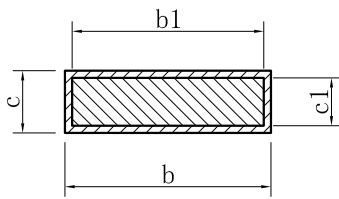
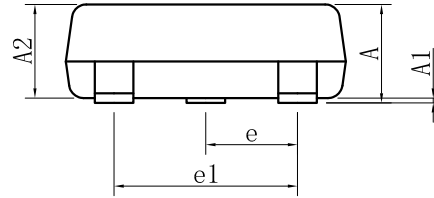
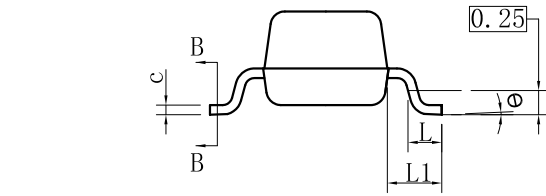
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Static					
Drain–Source Breakdown Voltage (VGS = 0 V, ID = 250 μA)	V(BR)DSS	100	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250 μA)	VGS(th)	1.0	-	3.0	V
Gate–Body Leakage (VDS = 0 V, VGS = ±20 V)	IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VDS= 100 V, VGS=0 V)	IDSS	-	-	1	μA
Static Drain–Source On–State Resistance(Note 3) (VGS = 10 V, ID = 3 A) (VGS = 4.5 V, ID = 1 A)	RDS(on)	- -	160 200	200 260	mΩ
Forward Voltage (VGS = 0 V, IS = 6.5 A)	VSD	-	0.9	1.3	V
Dynamic					
Total Gate Charge	(VDS =50V, VGS =5V, ID =6.5A)	Qg	-	5.8	nC
Gate–Source Charge		Qgs	-	2.0	
Gate–Drain Charge		Qgd	-	3.0	
Input Capacitance	(VDS =25V, VGS =0V, f=1MHz)	Ciss	-	501	pF
Output Capacitance		Coss	-	24.3	
Reverse Transfer Capacitance		Crss	-	19.6	
Turn-On Delay Time	(VDD =50V, RL =50Ω, VGEN =10V, RG =6.2Ω)	td(on)	-	7.98	ns
Rise Time		tr	-	4.85	
Turn-Off Delay Time		td(off)	-	11.1	
Fall Time		tf	-	5.4	

Note 3:Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

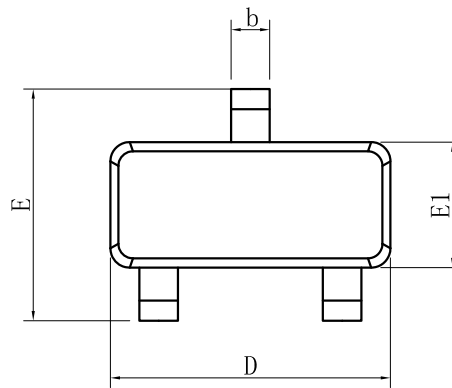
7. ELECTRICAL CHARACTERISTICS CURVES


7.ELECTRICAL CHARACTERISTICS CURVES(Con.)


7.ELECTRICAL CHARACTERISTICS CURVES(Con.)


8.OUTLINE AND DIMENSIONS


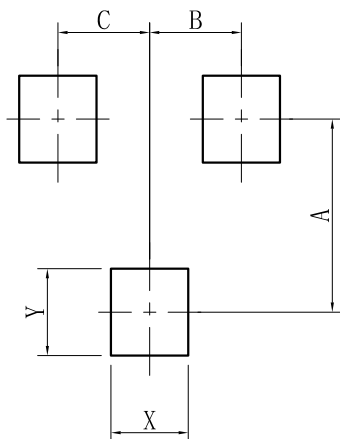
SECTION B-B



SOT23			
DIM	MIN	NOR	MAX
A	0.89	-	1.12
A1	0.01	-	0.10
A2	0.88	0.95	1.02
b	0.30	-	0.50
b1	0.30	0.40	0.45
c	0.08	-	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	-	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	-	8°
All Dimensions in mm			

GENERAL NOTES

- 1.Top package surface finish Ra0.4±0.2um
- 2.Bottom package surface finish Ra0.7±0.2um
- 3.Side package surface finish Ra0.4±0.2um

9.SOLDERING FOOTPRINT


SOT23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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