

LESD9L5.0CT5G

Transient Voltage Suppressors

ESD Protection Diodes with Ultra-Low Capacitance

The ESD9L is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free Device

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic

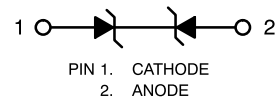
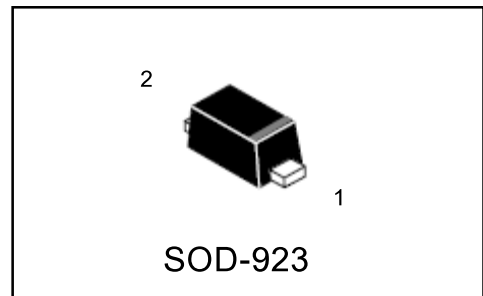
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

QUALIFIED MAX REFLOW TEMPERATUR : 260 °C

Device Meets MSL quireme

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Ordering information

Device	Marking	Shipping
LESD9L5.0CT5G	N	8000/Tape&Reel

Rating	Symbol	Value	Unit
IEC61000-4-2 Contact Air		±10	KV
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Temperature Range	T _J	-55 to +125	°C
Lead Solder Temperature-Maximum (10 Second Duration)	T _L	260	°C

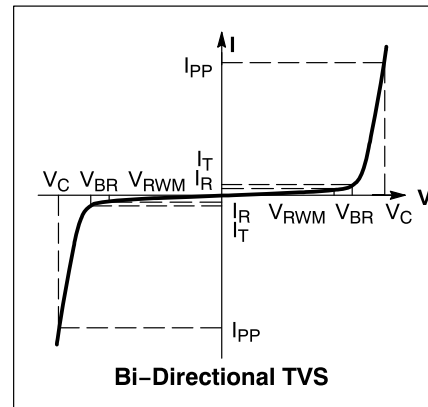
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
I _F	Forward Current
V _F	Forward Voltage @ I _F
P _{pk}	Peak Power Dissipation
C	Capacitance @ V _R = 0 and f = 1.0 MHz



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.0 V Max. @ I_F = 10 mA for all types)

Device	Device Marking	V _{RWM} (V)	I _R (μA) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	I _T (mA)	C (pF) (Max)	V _C (V) @ I _{PP} = 1 A (Note 3)	V _C (Per IEC61000-4-2 (Note 4))
		Max	Max	Min			Max	
LESD9L5.0CT5G	N	5.0	1.0	5.4	1.0	0.9	12.9	Figures 1 and 2 See Below

- V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
- Surge current waveform per Figure 5.
- For test procedure see Figures 3 and 4.

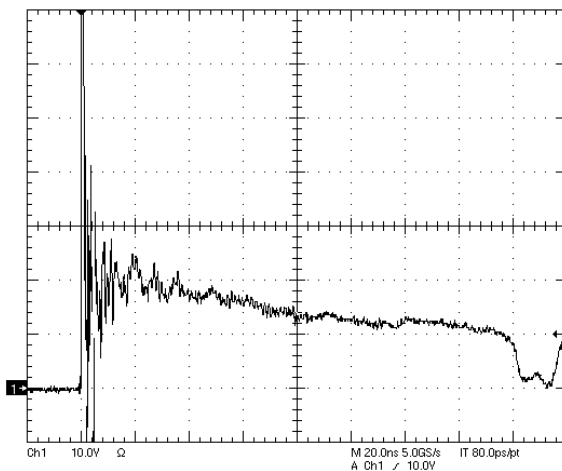


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

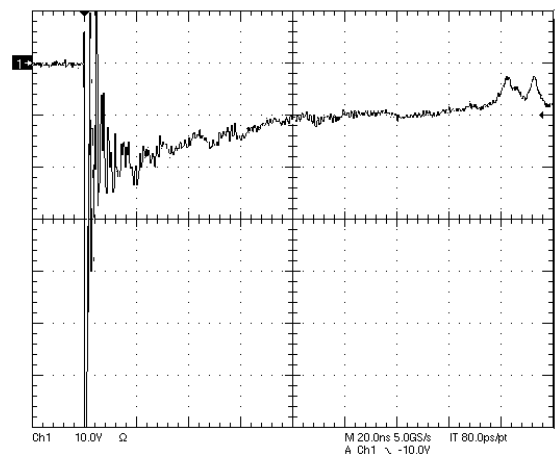


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

IEC61000-4-2 Waveform

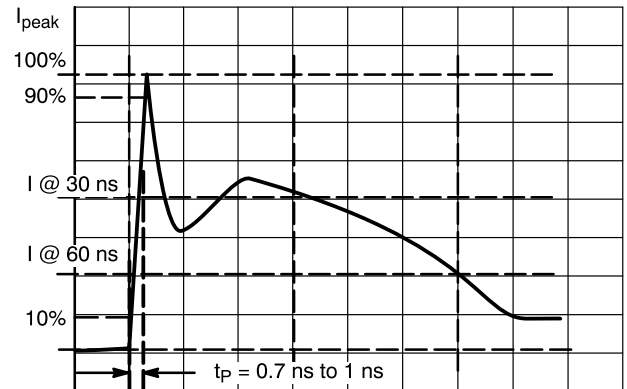


Figure 3. IEC61000-4-2 Spec

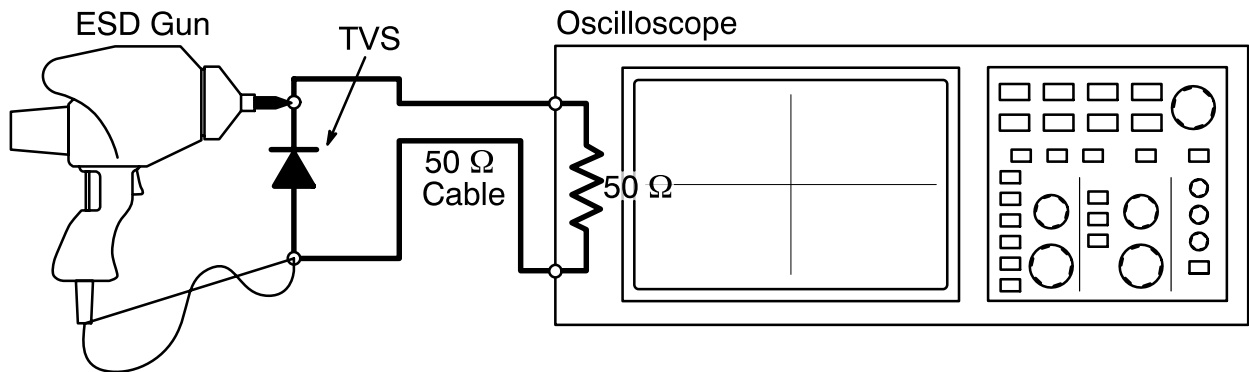


Figure 4. Diagram of ESD Test Setup

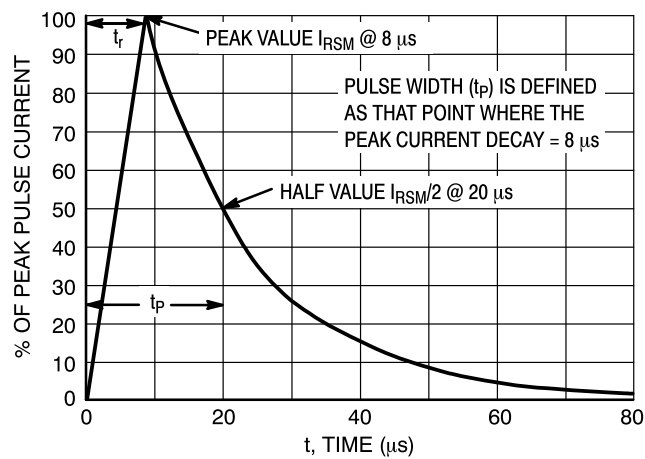
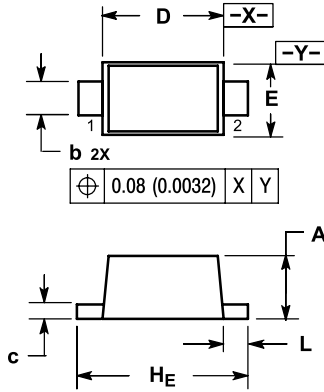


Figure 5. 8 X 20 μs Pulse Waveform

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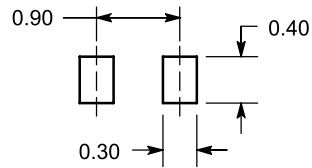
SOD-923



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
HE	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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